

SYSTEM AND CIRCUIT DESIGN TECHNIQUES FOR SILICON-BASED
MULTI-BAND/ MULTI-STANDARD RECEIVERS

A Dissertation

by

MOHAMED AHMED MOHAMED EL-NOZAH

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2010

Major Subject: Electrical Engineering

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Approved by:

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ABSTRACT

System and Circuit Design Techniques for Silicon-Based
Multi-Band/ Multi-Standard Receivers. (May 2010)

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Today, the advances in Complementary MetalOxideSemiconductor (CMOS) technology have guided the progress in the wireless communications circuits and systems area. Various new communication standards have been developed to accommodate a variety of applications at different frequency bands, such as cellular communications at 900 and 1800 MHz, global positioning system (GPS) at 1.2 and 1.5 GHz, and Bluetooth and WiFi at 2.4 and 5.2 GHz, respectively. The modern wireless technology is now motivated by the global trend of developing multi-band/multi-standard terminals for low-cost and multifunction transceivers. Exploring the unused 10-66 GHz frequency spectrum for high data rate communication is also another trend in the wireless industry.

In this dissertation, the challenges and solutions for designing a multi-band/multi-standard mobile device is addressed from system-level analysis to circuit implementation. A systematic system-level design methodology for block-level budgeting is proposed. The system-level design methodology focuses on minimizing the power consumption of the overall receiver. Then, a novel millimeter-wave dual-band receiver front-end architecture is developed to operate at 24 and 31 GHz. The receiver relies on a newly introduced concept of harmonic selection that helps to reduce the

complexity of the dual-band receiver. Wideband circuit techniques for millimeter-wave frequencies are also investigated and new bandwidth extension techniques are proposed for the dual-band 24/31 GHz receiver. These new techniques are applied for the low noise amplifier and millimeter-wave mixer resulting in the widest reported operating bandwidth in K-band, while consuming less power consumption.

Additionally, various receiver building blocks, such as a low noise amplifier with reconfigurable input matching network for multi-band receivers, and a low drop-out regulator with high power supply rejection are analyzed and proposed. The low noise amplifier presents the first one with continuously reconfigurable input matching network, while achieving a noise figure comparable to the wideband techniques. The low drop-out regulator presented the first one with high power supply rejection in the mega-hertz frequency range.

All the proposed building blocks and architecture in this dissertation are implemented using the existing silicon-based technologies, and resulted in several publications in IEEE Journals and Conferences.

To my Parents, Wife, Brother, Sister, and Daughter

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CHAPTER I

INTRODUCTION

Today, the advances in CMOS technology have guided the progress in the wireless communications circuits and systems area. Various new communication standards have also been developed to accommodate a variety of applications at different frequency bands, such as cellular communications at 900 and 1800 MHz, global positioning system (GPS) at 1.2 and 1.5 GHz, and Bluetooth and WiFi at 2.4 and 5.2 GHz, respectively. The modern wireless technology is now motivated by the global trend of developing terminals that support high data rate communication, and moving to the largely unused spectrum at millimeter-wave (mm-wave) frequencies while consuming less power consumption. Some system applications include IEEE 802.16 wireless metropolitan area network for point-to-point wireless communications at 10-66 GHz frequency range [1], automotive short-range and long range-radars at 22-29 GHz and 77 GHz, and cognitive radios [2, 3, 4, 5, 6, 7, 8].

With the existing variety of wireless standards, the idea of combining multiple bands is also very appealing for low giga-hertz and mm-wave frequencies. Combining several bands and standards into a single mobile unit faces many challenging problems including the design of reconfigurable or wideband RF front-ends and architectures to support multi-standard operation. Another important challenge in multi-band/multi-standard receiver implementation is that all the blocks usually share one or two supplies. The noise leaking through the supply of each building block may affect the functionality of the receiver. Hence, low drop-out regulators are important building blocks in this receivers to suppress the supply noise.

The journal model is *IEEE Journal of Solid-State Circuits*.

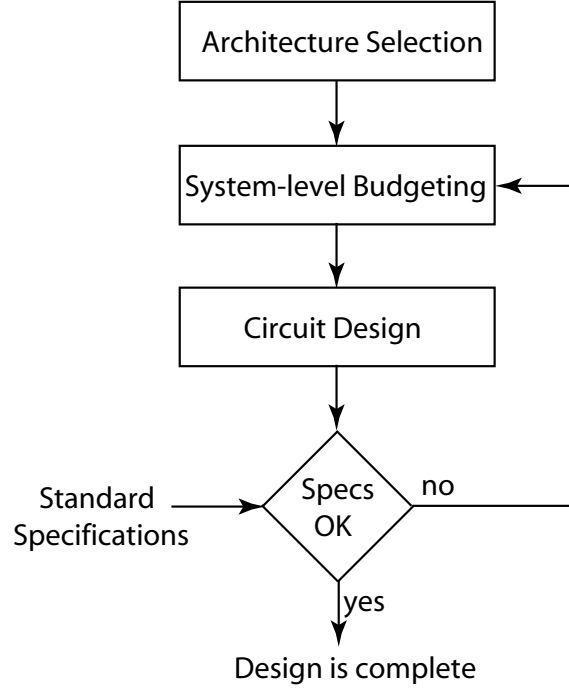


Fig. 1. Design steps for RF receiver.

Designing a mutli-band/multi-standard receiver includes several design steps. Fig. 1 summarizes these steps. In the first step, the proper architecture for the targeted application is selected. Then in step two, efficient system-level budgeting to minimize the overall power consumption is performed. The outcome of this step is the noise figure, linearity, and gain of each building block. Usually, system-level budgeting depends on the experience of the designer, and therefore a systematic approach is an important requirement in this step. Finally, reconfigurable or wideband circuits are designed to meet the system-level specifications. If the system-level specifications are not possible to be met by the circuit, system-level budgeting has to be repeated until all the specifications are satisfied. Each of these steps have its own challenges, and possible solutions are demonstrated in this dissertation.

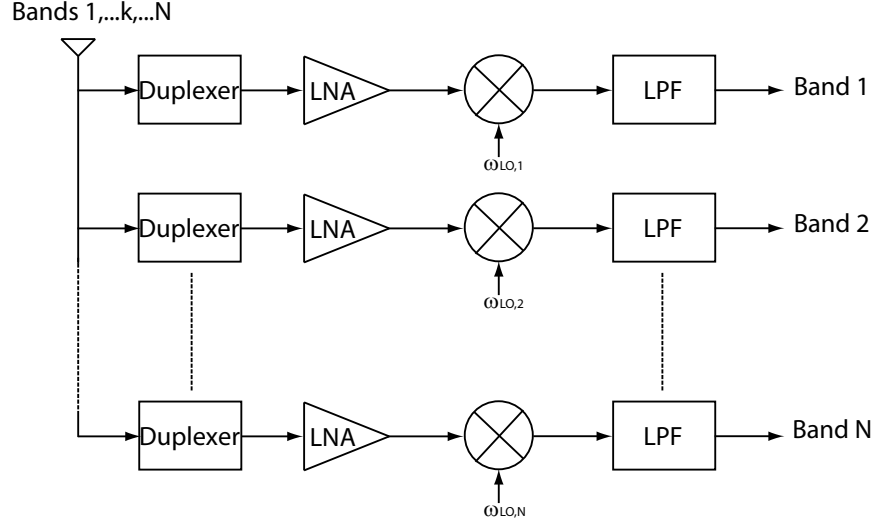


Fig. 2. Block diagram representation of a multi-band receiver using parallel architecture.

A. Existing Multi-Band/Multi-Standard Receiver Architectures

Several Multi-Band/Multi-Standard (MB/MS) receiver architectures have been proposed in the literature by means of parallel, weaver and concurrent architectures. The parallel architecture, shown in Fig. 2, utilizes several single-band architectures that are placed in parallel. Each branch is designed to receive one of the desired bands. Parallel receiver architectures are characterized by their low power consumption. However, due to the parallel path, the area consumption is high, which increases the cost of the chip after fabrication. In addition, layout is one of the challenges in the parallel receiver architecture design as the main target is to reduce the area. Parallel receiver approach has been reported for a variety of applications as follows: Zargari et al. [9] demonstrated a dual-band heterodyne CMOS receiver for 2.4/5.2-GHz wireless local area network (WLAN) applications using sliding IF architecture. Ko et al. [10] reported a CMOS 1.2/1.5-GHz dual-band heterodyne GPS receiver with

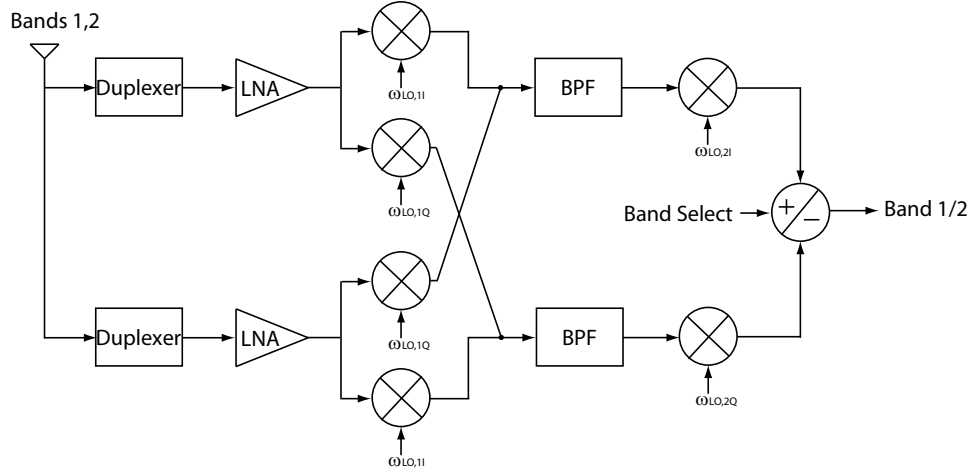


Fig. 3. Block diagram representation of a dual-band receiver using weaver architecture.

dual-conversion architecture. Finally, the first dual-band 22-29/77-81 GHz transceiver for automotive radars using direct conversion architecture is proposed in [11].

Using the weaver architecture, shown in Fig. 3, is another approach for dual-band reception that utilizes the image reject receiver. This architecture relies on the concept of placing the two bands as images of each other. Then, one of these two bands is selected and the other one is rejected using the image reject receiver. Wu et al. [12] was the first to report a weaver-based dual-band CMOS receiver at 900-MHz-1.8-GHz. This receiver architecture utilizes the same front-end for both bands, however, it increases the complexity of blocks operating at the RF frequency range including the low noise amplifier and RF mixer. It requires four RF mixers and two IF ones. This complexity increases the power and area consumption of the receiver.

Concurrent reception is another technique used for dual-band reception as shown in Fig. 4 [13]. In this architecture, both bands are received concurrently. Chen et al. [14] introduced this receiver architecture for GPS and Bluetooth applications. A dual-band low noise amplifier is used to reduce the area consumption of the receiver.

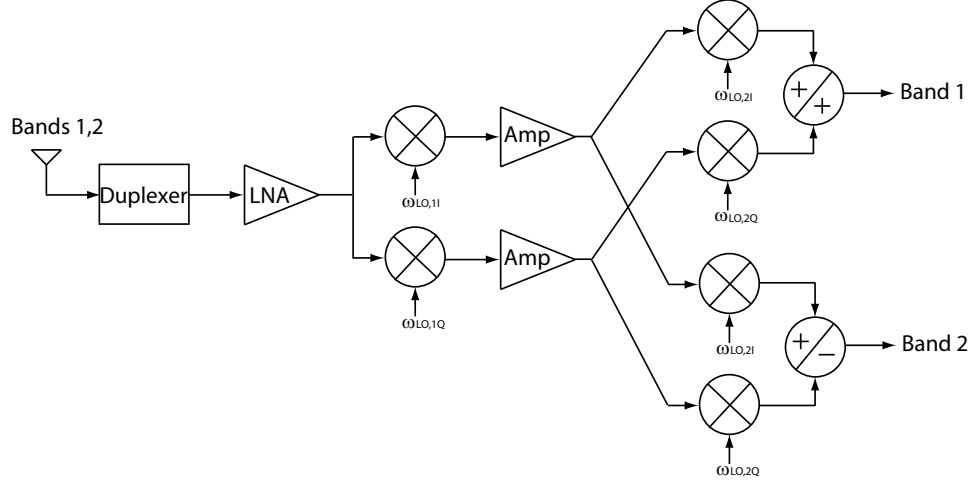


Fig. 4. Block diagram representation of a dual-band receiver using concurrent architecture.

The main challenge in this architecture is the increased complexity at the IF blocks.

In summary, the design of multi-band (dual-band) receiver started initially with parallel-based architectures. Then, several techniques are introduced to reduce the area of the receiver by reusing the building blocks through weaver and concurrent reception. Utilizing the weaver or concurrent receiver architectures at mm-wave frequencies is challenging because the increased complexity of the RF section (low noise amplifier and mixer) may degrade the performance of the receiver severely compared to low giga-hertz applications.

B. System-level Budgeting

Poor system-level design can result in considerable waste of power and chip area. Usually, system-level design can be divided into three main steps: 1) overall system-level specification estimation; 2) frequency planning; and 3) block-level budgeting. The third step requires several manual iterations to find the optimum set of specifications

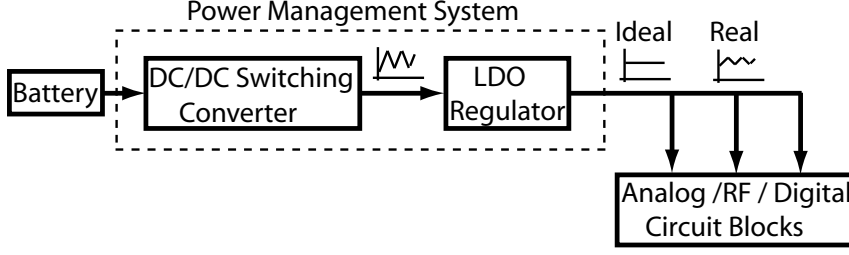


Fig. 5. Block diagram of typical power management system.

(including the input-referred noise and nonlinearity) for each building block. However, it is not guaranteed that the final set of specifications for each block minimizes power consumption. A block-level budgeting methodology for single-band-single-standard (SB-SS) receivers has been proposed to minimize power consumption in [15]. This methodology introduces a new systematic approach to determine performance parameters (noise figure, and input referred third order intercept point) of each building block. However, this methodology can not be applied directly for MB-MS receivers because it neglects the dependency of the performance parameters on the operating frequency. This problem is addressed through the work done in this dissertation.

C. Power Management Unit in Receivers

Another important building block in the wireless receiver is the low drop-out (LDO) regulator in the power management unit, shown in Fig. 5. The LDO regulator is used to regulate supply ripples to provide a clean voltage source for the noise-sensitive analog/RF blocks. Designing a stable LDO for a wide range of load condition, while achieving high power supply-rejection (PSR), low drop-out voltage, and low quiescent current, is an important requirement for the state-of-the-art wireless transceivers [16, 17, 18]. The main reason for poor PSR at high frequencies is the

finite output conductance of the pass transistors, and low DC gain of the newer technologies. Designing an LDO with high PSR up to few mega-hertz frequencies to cope with the increasing frequency of the integrated switching converter is an important requirement in the state-of-art receivers, and therefore this block is addressed for the multi-band/multi-standard receiver.

D. Summary of Challenges in Multi-Band/Multi-Standard Receivers

The main goal in these receiver architectures is to share as many building blocks as possible for various standards to reduce the cost and area of the handheld devices. Implementing dual/multi-band receivers operating at low giga-hertz or mm-wave frequencies faces many challenging problems including:

- Challenge 1: Good system-level design methodology has to be developed to reduce the overall power consumption,
- Challenge 2: New architectures have to be developed with the focus of reducing the complexity and power consumption,
- Challenge 3: Front-end building blocks including LNA and mixer have to support very wide frequency range,
- Challenge 4: Front-end building blocks have to be reconfigurable,
- Challenge 5: Low drop-out voltage regulators have to achieve high power supply rejection.

E. Objective of Dissertation

The primary goals of this thesis are to investigate and to provide solutions for the challenging problems facing multi-band/multi-standard receivers. Objectives of this

work are summarized as follows:

- To develop an optimum MB/MS system-level design methodology targeting low power consumption:

The aim is to develop a methodology that determines specifications (noise figure (NF), gain and linearity) for each building block to minimize the overall power consumption for a multi-band/ multi-standard (MB/MS) receiver. Analytical expressions for the optimum gain, NF, and input-referred third-order intercept point of each building block needs to be developed. Finally, the design methodology has to be verified for some of the existing standards showing the advantage of the proposed methodology. (Challenge 1)

- To propose a new receiver architecture for MB mm-wave receivers:

The goal is to propose a new dual-band millimeter-wave receiver architecture for down-converting the ISM (Industrial, Scientific, Medical) and LMDS (Local Multipoint Distribution Service) bands at 24 and 31 GHz. Compared to previous architectures, the proposed front-end has to utilize the same building blocks for the two bands, and has to reduce the operating frequency of the local oscillators; thereby reducing the total area consumption. Mathematical analysis, frequency planning and system budgeting need to be examined. Finally, implementing a prototype is part of the work to show the proper operation of the receiver. (Challenge 2)

- To propose wideband circuit techniques for mm-wave front-ends:

The target of this objective is to develop wideband circuit techniques for the mm-wave LNA and mixer for the proposed dual-band 24/31 GHz receiver architecture. Proposed approaches should target low power consumption while providing a low noise figure and high third order intercept point to cope with

IEEE 802.16 wireless standard. Electromagnetic simulation setups of passive components and routings between devices are necessary to provide an accurate modeling of the actual circuit behavior. Finally, a prototype implementation for each building block to check the wideband operation of proposed circuits is another target. (Challenge 3)

- To propose a new reconfigurable low noise amplifier architecture:

The reconfigurable low noise amplifier (LNA) has to provide a continuously tunable input matching network to reduce the linearity requirement of the RF front-end. Analytical expressions for the performance parameters have to be developed to understand the functionality of the proposed technique. Finally, a design methodology needs to be presented to be a design guideline for future prototypes. The targeted frequency range is 1.9-2.4 GHz, which is the frequency range of many wireless standards. A prototype should be implemented to test the functionality of the proposed LNA. (Challenge 4)

- To propose a new low drop-out regulator with high power supply rejection:

The aim is to design a new architecture that provides high power supply rejection up to few mega-hertz frequencies. Complete analysis and design steps of the proposed technique are necessary as part of the work. Effect of external parasitics such as bonding wires and traces should be addressed in this work. A prototype need to be implemented to verify the functionality of the proposed technique. (Challenge 5)

F. Dissertation Organization

The dissertation consists of six chapters organized as follows

Chapter II presents a new design methodology for MB-MS CMOS receivers.

Closed-form analytical expressions are presented for the system-level specifications to speed up the design cycle. The methodology is applied for system-level budgeting of a MB-MS receiver for mobile communications (GSM) 900- and 1900-MHz bands, global positioning systems (GPS), and wideband code-division multiple-access (WCDMA) standards.

Chapter III demonstrates the implementation of a new dual-band switchable harmonic receiver architecture (SWHR) to down-convert the ISM and LMDS bands at 24 and 31 GHz, respectively. The receiver is targeting IEEE-802.16 single carrier standard. The frequency planning and mathematical formulation of the proposed architecture are also presented. In addition, new wideband circuit techniques for mm-wave front-ends of the receiver are demonstrated. Finally, measurement results for individual building blocks and whole receiver is provided through a fabricated prototype using Jazz 0.18 μm BiCMOS technology.

In Chapter IV, a new continuously reconfigurable LNA is presented. The proposed LNA relies on a new technique to continuously tune the inductance value. The detailed analysis of the proposed LNA, including the tuning range and additional noise of the proposed reconfigurable input matching network, is also presented. Measurement results of a prototype using 0.13 μm CMOS technology for the 1.9-2.4 GHz frequency range is performed.

Chapter V explains a novel feed-forward ripple cancellation (FFRC) technique to achieve high PSR low-voltage LDO regulator. The mathematical analysis of the proposed technique and the effect of finite power supply rejection ratio of the amplifier on the PSR of the LDO are developed. The effect of bonding wires are also investigated in this chapter. Measurement results of a fabricated prototype using 0.13 μm CMOS technology is provided to verify the functionality of the proposed technique.

Finally, Chapter VI concludes the discussion about the proposed design tech-

niques, novel dual-band receiver architecture, and high-performance building blocks presented in this dissertation.

G. Major Contributions of This Dissertation

The thesis explores design and implementation methodologies for MB-MS mobile units that target high data rate while consuming minimum power consumption. The thesis covers various aspects of MB-MS receivers and their building blocks including system-level design [19, 20], novel architectures of the receiver, wideband building blocks for mm-wave frequency range [21], a reconfigurable low noise amplifier [22], and a low-drop out regulator with high power supply rejection [23, 24]. The research methodology promises significant improvement in power budget and is realizable by the aid of low-cost silicon-based technologies.

A new dual-band receiver architecture that reduces the front-end complexity at mm-wave frequencies provides a new technique for dual-band reception through switchable harmonic mixing. The new architecture can be used at low giga-hertz frequency range as well. The presented wideband circuit techniques present novel approaches to increase the bandwidth of silicon-based building blocks at mm-wave frequencies. These approaches sustain the performance of the building blocks in-spite of increasing the bandwidth.

The new inductance scaling scheme for the low noise amplifier with reconfigurable input matching network demonstrates the approach to continuously tune the input matching network for the first time. In addition, the inductance scaling scheme can be used in other circuit implementations that target low-noise performance.

Finally, the proposed feed-forward technique demonstrates a novel approach to increase the bandwidth of supply rejection of the low drop-out regulator. This tech-

nique shows a supply rejection better than 56 dB up to 10 MHz, presenting the widest reported supply rejection bandwidth.

Successful demonstration of the various ideas and techniques presented in this thesis invokes huge commercial interest. This is due to the enormous cost and size reduction of traditional reconfigurable receivers previously used in military, navigation, remote sensing and satellite communications at these frequencies. Many commercial products with large scale markets can benefit from proposed solutions. Cellular communications infrastructures, broadband services such as voice, data, video and internet, and long-range, short-range automotive collision avoidance radars are some of the applications. Additionally, this work demonstrates the feasibility of using low speed silicon-based technologies to implement mm-wave circuits and systems in spite of their low cut-off frequencies, and large parasitics compared to traditional high quality but expensive III-V technologies.

CHAPTER II

SYSTEM-LEVEL DESIGN METHODOLOGY FOR MULTI-BAND/MULTI-STANDARD RECEIVERS

A. Introduction

The current trend of wireless communication systems and circuits has driven the industry to develop multi-band and multi-standard (MB-MS) mobile units. With cellular phones operating from 800 MHz to 1.9 GHz, the global positioning system (GPS) at 1.2 and 1.5 GHz, the wireless personal area network (WPAN) from 400 MHz to 10 GHz, and the wireless area network (WLAN) at 2.4, 5.2 and 5.8 GHz, it has been desirable to combine more than one band/standard in the same mobile unit, to reduce the complexity and power consumption [9, 12, 25, 26].

High performance MB-MS mobile unit implementation faces many challenges including the required higher level of integration, lower power consumption, and efficient frequency planning. All these challenges have been the main focus of many proposed MB-MS receiver architectures [9, 12, 25, 26]. In addition, poor system-level design can result in considerable waste of power and chip area. Usually, system-level design can be divided into three main steps: (1) overall system-level specification estimation (such as the overall noise figure and linearity requirements), (2) frequency planning, and (3) block-level budgeting. The third step requires several manual iterations in order to find the optimum set of specifications (including the input referred noise and non-linearity) for each building block. However, it is not guaranteed that the final set of specifications for each block minimizes the power consumption. A block-level budgeting methodology for a single-band/single-standard (SB-SS) receiver has been proposed in [15] to minimize the power consumption of the receiver. However to our

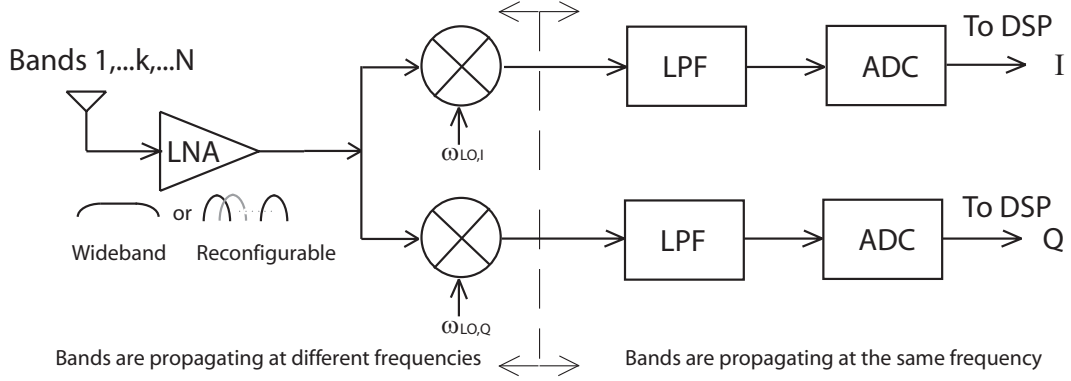


Fig. 6. A multi-band/multi-standard direct conversion receiver. The bands are propagating at different (same) frequencies before (after) the RF mixer.

knowledge, a methodology that can be applied to a general MB-MS receiver has not been proposed.

In this chapter, a generalized methodology for system-level budgeting of MB-MS receivers to minimize the power consumption is presented. A reconfigurable or wideband LNA is employed to cover different frequency bands while mixer and baseband sections are shared for different bands and standards (Fig. 6) as in current MB-MS systems. Having several (parallel) LNAs will give an additional flexibility to optimize the receiver chain. However, the same receiver chain (single wideband/reconfigurable LNA) is considered because the current trend goes for higher level of integration by reusing various receiver building blocks [9, 12, 25, 26]. It is important to note that the gain, noise figure (NF) and input referred third order intercept point ($IIP3$) of the mixer and baseband blocks are the same for all bands because RF signals are down-converted to the same spectrum.

This chapter starts with a background section discussing the various performance specifications of the RF receiver and the SB-SS approach for minimizing the power consumption is discussed. Then, a system-level design example for a dual-band re-

ceiver is presented to highlight the difficulty of the block-level budgeting of MB-MS receiver. Finally, the generalized methodology is demonstrated at the end of this chapter.

B. Background

In this section, the estimation of overall system-level specification starting from the standard are initially discussed. Then, analytical expression for the basic building blocks of the CMOS RF receiver are presented. These analytical expression help to establish the proposed system-level design methodology.

1. RF Receiver System-Level Specifications

Overall system-level specifications are usually calculated from the bit error rate (BER) requirements specified in the standard. The BER is then translated to the signal to noise ratio (SNR), from which the NF and $IIP3$ are calculated. Depending on the channel conditions, modulation scheme, error correction, and channel coding the SNR at the output, SNR_o , of the receiver is determined from [27]

$$SNR_o = \frac{E_b}{N_o} \frac{R}{NEB}, \quad (2.1)$$

where E_b is the energy per information bit, N_o is the noise power spectral density, R is the bit rate in bps, and NEB is the noise-equivalent bandwidth. The SNR_o in (2.1) represents a lower limit for the receiver design, and usually an additional margin that accounts for additional non-idealities such as process variations, and phase noise of the synthesizer is added. The overall noise figure, NF_{ov} , and third order input

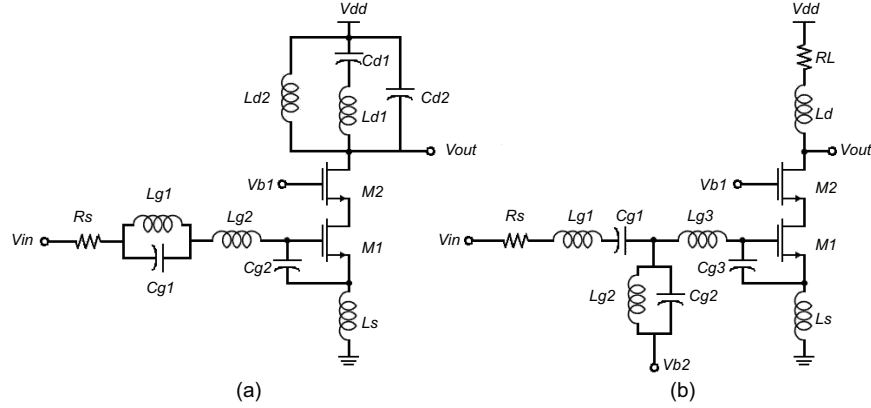


Fig. 7. (a) Common Source Concurrent LNA (b) wide band LNA.

intercept point, $V_{IIP3,ov}^2$, of the receiver are found from [15, 28]

$$NF_{ov} = P_{mds} - 10\log(KTB) - SNR_o, \quad (2.2)$$

$$V_{IIP3,ov}^2 = \frac{3P_{mds} - NF_{ov} - 10\log(KTB)}{2}, \quad (2.3)$$

where P_{mds} is the minimum detectable signal, K is the Boltzmann constant, T is the temperature in Kelvin, and B is the channel bandwidth. Usually, (2.3) is defined by the standard and may differ from one standard to the other one.

2. Building Blocks Performance Specifications

In this part of the section, analytical expressions of the performance parameters for the various basic building blocks of CMOS receiver are derived. These expressions will provide a guideline for the proposed design methodology.

a. Low Noise Amplifier

Common source LNAs with inductive source generation have been used for narrow band RF front-ends frequently [28, 29]. For the dual/multi-band systems, parallel,

concurrent, or wideband LNAs, as shown in Fig. 7, can be used [30]. Assuming perfect matching at two different bands, the input referred noise, input referred third order intercept point, and gain of a narrow-band LNA are [15, 31]

$$\bar{V}_{ni}^2 = 4KT\gamma g_{m1}R_s^2\left(\frac{\omega_o}{\omega_T}\right)^2, \quad (2.4)$$

$$V_{IIP3}^2 = \frac{16}{3}\frac{I}{\theta}g_{m1}R_s^2\left(\frac{\omega_o}{\omega_T}\right)^2, \quad (2.5)$$

$$A = \frac{R_L}{2R_s}\frac{\omega_T}{\omega_o}, \quad (2.6)$$

where K is the Boltzmann's constant, T is the temperature, γ is a noise factor, ω_o is the operating frequency, ω_T is the cut-off frequency of the transistor, I is the DC current, θ is a parameter to account for mobility degradation, and R_s and R_L are the source and load resistances, respectively.

Two important observations are concluded from the analytical expressions in eqs. (2.4) to (2.6). The first one is the proportionality of the dynamic range, DR_{LNA} , to the biasing current and hence the power consumption, P [15]

$$DR_{LNA} = \frac{V_{IIP3}^2}{\bar{V}_{ni}^2} = \frac{4}{3KT\gamma\theta}I = \frac{P}{P_{c,LNA}}, \quad (2.7)$$

where $P_{c,LNA}$ is a proportionality coefficient that relates the DR_{LNA} to the power consumption and is technology dependent. The supply voltage did not appear in the DR_{LNA} because the input signal is assumed to be small, and hence, the linearity of the device determines V_{IIP3}^2 . It is important to note that the DR_{LNA} is independent of the operating frequency.

The second observation is the dependency of performance parameters of the LNA on the operating frequency. For single-band receiver, this dependency is not a problem because the receiver is designed at a specific frequency. However, for dual/multi-band systems, the gain, NF , and $IIP3$ of the LNA are frequency dependent. This

frequency dependency is the main challenge for minimizing the power consumption. This is because the worst NF and $IIP3$ should be considered during the block-level budgeting. Similar conclusion can be obtained for the concurrent and wideband LNA architectures.

b. RF Mixer

A single- or double-balanced mixer is commonly used in RF receivers. For a double-balanced Gilbert cell mixer, the total input referred noise, input referred third order intercept point, and gain are calculated from [32, 33]

$$\bar{V}_{ni}^2 \approx 2\pi^2 KT \frac{\gamma}{g_{m1}}, \quad (2.8)$$

$$V_{IIP3}^2 = \frac{16}{3} \frac{v_{sat} L}{(\mu_o + 2v_{sat}\theta L)} V_{od} \approx \frac{16}{3} \frac{I}{\theta g_{m1}}, \quad (2.9)$$

$$A = \frac{2}{\pi} g_{m1} R_L. \quad (2.10)$$

where L is the channel length, v_{sat} is the saturation voltage, μ_o is the mobility, and V_{od} is the overdrive voltage.

Similar to the LNA, the dynamic range of the mixer depends on the biasing current but with a different mixer power coefficient, $P_{c,mixer}$. In this case, the dynamic range, DR_{mixer} , of the mixer is given by

$$DR_{mixer} = \frac{V_{IIP3}^2}{\bar{V}_{ni}^2} = \frac{8}{3\pi^2 KT \gamma \theta} I = \frac{P}{P_{c,mixer}}, \quad (2.11)$$

$P_{c,mixer}$ is also technology dependent and it relates the DR_{mixer} to the power consumption. As depicted in the set of equations from (2.8) to (2.11), none of the parameters depends on the frequency. However, internal nodes parasitic capacitances can change this dependency when the operating frequency is very high such as in millimeter-wave applications. In the following analysis, the frequency dependency is

neglected as low giga-hertz receivers are considered. However, similar analysis could be conducted if the internal node parasitic capacitances are effective.

c. Second Mixing and Baseband Stages

The remaining blocks of the RF receiver could be a second mixing stage followed by baseband processing in an IF receiver or the baseband section in the low-IF for direct conversion receivers. Sheng et al. proved that baseband circuits also have a dynamic range that is proportional to the power consumption [15], and the same postulate is used for all the building blocks through the rest of this analysis.

3. Overall System-Level Specifications

For a cascaded receiver, similar to the one shown in Fig. 6 (either homodyne or heterodyne one), the overall performance specifications $(NF_{ov}, V_{IIP3,ov}^2)$ are obtained based on Friis equation for the overall noise figure and linearity [34]. For integrated RF receivers the assumption of conjugate match is not the case, and therefore Friis equation is modified to include the voltage gain and input referred noise voltage instead of the power gain and noise figure. The resultant overall performance in terms of the individual block-level specifications is as follows [28]

$$(NF_{ov}(\omega) - 1)KT = \sum_{i=1}^n a_i(\omega), \quad \frac{1}{V_{IIP3,ov}^2(\omega)} = \sum_{i=1}^n b_i(\omega),$$

$$a_i(\omega) = \begin{cases} \bar{V}_{ni,i}^2 & \text{if } i = 1 \\ \frac{\bar{V}_{ni,i}^2}{\prod_{j=1}^{i-1} A_j^2} & \text{if } i > 1 \end{cases}, \quad b_i(\omega) = \begin{cases} \frac{1}{V_{IIP3,i}^2} & \text{if } i = 1 \\ \frac{\prod_{j=1}^{i-1} A_j^2}{V_{IIP3,i}^2} & \text{if } i > 1. \end{cases} \quad (2.12)$$

where the subscript i is the block number, n is the total number of blocks, the subscript ov stands for the overall system performance, and $\bar{V}_{ni,i}^2$, $V_{IIP3,i}^2$, and A_i are the input referred noise voltage, input referred third order intercept point and the

gain of the i^{th} block, respectively.

4. Block-Level Budgeting of a SB-SS Receiver

For a SB-SS CMOS receiver, Sheng et al. proved that minimum power consumption is achieved when $\overline{V_{ni,i}^2}$ and $V_{IIP3,i}^2$ are calculated from [15]

$$\overline{V_{ni,i}^2} = \begin{cases} \frac{(NF_{ov}-1)kT \cdot 50 \sqrt[3]{P_{c,i}}}{\sum_{j=1}^n \sqrt[3]{P_{c,j}}} & \text{if } i = 1 \\ \frac{(NF_{ov}-1)kT \cdot 50 \sqrt[3]{P_{c,i}}}{\sum_{j=1}^n \sqrt[3]{P_{c,j}}} \prod_{j=1}^{i-1} A_j^2 & \text{if } i > 1 \end{cases} \quad (2.13)$$

$$V_{IIP3,i}^2 = \begin{cases} V_{IIP3,ov}^2 \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,i}}} & \text{if } i = 1 \\ V_{IIP3,ov}^2 \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,i}}} \prod_{j=1}^{i-1} A_j^2 & \text{if } i > 1 \end{cases} \quad (2.14)$$

Eqs. (2.13) and (2.14) show that blocks with higher P_c have relaxed specification to reduce the overall power consumption. Also, these equations do not provide sufficient information about the gain of each block. For SB-SS receiver, the gain is considered as a degree of freedom [15], and does not affect the overall power consumption. The power consumption is mainly determined by the noise figure and linearity of the block. The gain can be adjusted by changing the load resistance. However, for MB-MS receivers gain is an important parameter that affects the overall power consumption, as shown later in this chapter.

The minimum power consumption of the SB-SS receiver is found using (2.13) and (2.14), and is given by

$$P_{ov,min} = \sum_{j=1}^n P_{c,j} \cdot DR_j = \frac{V_{IIP3,ov}^2}{(NF_{ov}-1)kT \cdot 50} \left(\sum_{j=1}^n \sqrt[3]{P_{c,j}} \right)^3. \quad (2.15)$$

Eq. (2.15) points out that $P_{ov,min}$ depends on the overall DR of the receiver and also power coefficients of different building blocks. For MB-SS receivers, the dependency of performance parameter of the LNA makes the gain of the LNA an important

parameter that should be controlled to minimize power consumption. In following analysis, it is proven that *there is an optimum gain variation of the LNA at different bands/standards to achieve the minimum power consumption in MB-MS receivers.*

C. Budget Distribution for Dual-Band Receivers

Two different cases for block-level budgeting of DB-SS receiver are considered. In the first one, the gain of the LNA is assumed to decrease with the operating frequency as demonstrated by (2.6). In the second one, an LNA with constant gain is assumed. In both of these cases, block-level specifications for minimum power consumption are calculated.

1. Conditions for Minimum Power Consumption

The overall power consumption, P_{ov} , of the dual-band RF receiver is obtained by the summation of the power consumption of each building block, hence

$$P_{ov} = \sum_{i=1}^n P_{c,i} D R_i = \text{constant}. \quad (2.16)$$

As indicated by (2.16), the power consumption is independent of the operating frequency, and therefore, the overall power consumption for the two bands is the same.

Similar analysis to [15] has been conducted to find the optimum conditions for minimum power consumption. A constraint optimization problem is solved using Lagrange Multipliers, where the power consumption, defined in (2.16), is the dependent variable to be minimized, the overall NF_{ov} and $V_{IIP3,ov}^2$ are the constraints, and the input referred noise voltage and input referred third order intercept point of each building block are the independent variables. As a result, the input referred noise

voltage and $IIP3$ of each block are as follows

$$\bar{V}_{ni,i}^2 = \begin{cases} \frac{(NF_{ov}(\omega)-1)KT \cdot 50 \sqrt[3]{P_{c,i}}}{\sum_{j=1}^n \sqrt[3]{P_{c,j}}} & \text{if } i = 1 \\ \frac{(NF_{ov}(\omega)-1)KT \cdot 50 \sqrt[3]{P_{c,i}}}{\sum_{j=1}^n \sqrt[3]{P_{c,j}}} \prod_{j=1}^{i-1} A_j^2 & \text{if } i > 1 \end{cases} \quad (2.17)$$

$$V_{IIP3,i}^2 = \begin{cases} V_{IIP3,ov}^2(\omega) \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,i}}} & \text{if } i = 1 \\ V_{IIP3,ov}^2(\omega) \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,i}}} \prod_{j=1}^{i-1} A_j^2 & \text{if } i > 1 \end{cases} \quad (2.18)$$

Eqs. (2.17) and (2.18) show conditions for the input referred noise voltage and $IIP3$ of each building block for minimum power consumption. However, these equations do not provide sufficient information about values of the gain of building blocks for minimum power consumption. For a single-band receiver, gain is considered a degree of freedom [15]. This is not the case for a dual-band system, as shown below. To emphasize the importance of gain, two cases are considered. The first one considers an LNA with decreasing gain versus frequency, and the second one considers an LNA with a constant gain frequency response.

2. Design Case 1: Gain of LNA is Decreasing with the Frequency

This case assumes that the load resistance and power consumption for the two bands are the same for the LNA. As a result, the NF , $IIP3$ and gain of the LNA are frequency dependent as shown earlier in (2.4) to (2.6). Substituting these equations in (2.12), the NF_{ov} and $V_{IIP3,ov}^2$ are reduced to

$$\begin{aligned} (NF_{ov}(\omega) - 1)KT \cdot 50 &= (\bar{V}_{ni,LNA}^2(\omega_1) + \frac{\bar{V}_{ni,Mixer}^2}{A_{LNA}^2(\omega_1)} \\ &+ \frac{\bar{V}_{ni,Filter}^2}{A_{LNA}^2(\omega_1)A_{mixer}^2} + \dots) \left(\frac{\omega}{\omega_1}\right)^2, \end{aligned} \quad (2.19)$$

$$\begin{aligned} \frac{1}{V_{IIP3,ov}^2(\omega)} &= \left(\frac{1}{V_{IIP3,LNA}^2(\omega_1)} + \frac{A_{LNA}^2(\omega_1)}{V_{IIP3,Mixer}^2} \right. \\ &\quad \left. + \frac{A_{LNA}^2(\omega_1)A_{Mixer}^2}{V_{IIP3,Filter}^2} + \dots \right) \left(\frac{\omega_1}{\omega} \right)^2, \end{aligned} \quad (2.20)$$

where $A_{LNA}(\omega_1)$ is the gain of the LNA at the first frequency band. Eqs. (2.19) and (2.20) indicate that the lower frequency band have better overall noise figure on the cost of worse linearity when compared to the higher band. Hence, during the budget distribution, the required noise figure, defined in (2.12), should be monitored for the upper frequency band, while the non-linearity, defined in (2.12), should be considered for the lower frequency band. As a result, a lower noise figure and higher linearity is obtained at lower and upper bands, respectively. This condition increases the dynamic range of the receiver leading to an increase in the overall power consumption. The overall noise figure, IIP3 and power consumption at the two bands are

$$NF_{ov}(\omega_1) = 1 + (NF_{ov}(\omega_2) - 1) \left(\frac{\omega_1}{\omega_2} \right)^2, \quad (2.21)$$

$$NF_{ov}(\omega_2) = P_{mds} - 10 \log(KTB) - SNR_o, \quad (2.22)$$

$$V_{IIP3,ov}^2(\omega_1) = \frac{3P_{mds} - NF_{ov} - 10 \log(KTB)}{2}, \quad (2.23)$$

$$V_{IIP3,ov}^2(\omega_2) = V_{IIP3,ov}^2(\omega_1) \left(\frac{\omega_2}{\omega_1} \right)^2, \quad (2.24)$$

$$P_{ov} = \frac{V_{IIP3,ov}^2(\omega_1)}{(NF_{ov}(\omega_2) - 1)KT \cdot 50} \left(\sum_{j=1}^n \sqrt[3]{P_{c,j}} \right)^3 \left(\frac{\omega_2}{\omega_1} \right)^2. \quad (2.25)$$

Note that in the above equations, $NF_{ov}(\omega_2)$ and $V_{IIP3,ov}^2(\omega_1)$ are defined in the standard. On the other hand, $NF_{ov}(\omega_1)$ and $V_{IIP3,ov}^2(\omega_2)$ are estimated based on (2.21) and (2.24), respectively. Also, the above result in (2.25) points out that the dynamic range of the blocks increases as the two frequency bands are placed further apart. As a result, the total power consumption increases. In the following part, it is shown that power consumption may be decreased if the gain behavior of the LNA versus frequency is kept constant.

3. Design Case 2: Constant Gain Response of the LNA

In this case, a constant gain of the LNA for the two bands is considered. Constant gain can be achieved by adjusting the value of R_L , which to a first order approximation does not change the NF and $IIP3$ of the block. Under the assumption of constant gain response of the LNA, eqs. (2.19) and (2.20) are modified to

$$(NF_{ov}(\omega) - 1)KT \cdot 50 = (\bar{V}_{ni,LNA}^2(\omega_1)(\frac{\omega}{\omega_1})^2 + \frac{\bar{V}_{ni,Mixer}^2}{A_{LNA}^2(\omega_1)} + \frac{\bar{V}_{ni,Filter}^2}{A_{LNA}^2(\omega_1)A_{mixer}^2} + \dots), \quad (2.26)$$

$$\frac{1}{V_{IIP3,ov}^2(\omega)} = (\frac{1}{V_{IIP3,LNA}^2(\omega_1)}(\frac{\omega_1}{\omega})^2 + \frac{A_{LNA}^2(\omega_1)}{V_{IIP3,Mixer}^2} + \frac{A_{LNA}^2(\omega_1)A_{mixer}^2}{V_{IIP3,Filter}^2} + \dots). \quad (2.27)$$

For this case, the contribution of NF and $IIP3$ of the blocks that follow the LNA remains the same, and is independent of the frequency band. The constant gain case is the commonly used case for the system-level design of the dual-band RF CMOS receivers because it reduces the power consumption. For this case, eqs. (2.21), (2.24), and (2.25) are changed to

$$NF_{ov}(\omega_1) = 1 + (NF_{ov}(\omega_2) - 1) \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,1}}(\frac{\omega_2}{\omega_1})^2 + \sum_{j=2}^n \sqrt[3]{P_{c,j}}}, \quad (2.28)$$

$$V_{IIP3,ov}^2(\omega_2) = V_{IIP3,ov}^2(\omega_1) \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,1}}(\frac{\omega_1}{\omega_2})^2 + \sum_{j=2}^n \sqrt[3]{P_{c,j}}}, \quad (2.29)$$

$$P_{ov} = \frac{V_{IIP3,ov}^2(\omega_1)}{(NF_{ov}(\omega_2) - 1)KT \cdot 50} \frac{(\sum_{j=1}^n \sqrt[3]{P_{c,j}})^4}{\sqrt[3]{P_{c,1}}(\frac{\omega_1}{\omega_2})^2 + \sum_{j=2}^n \sqrt[3]{P_{c,j}}}. \quad (2.30)$$

Note that in the above equations, $NF_{ov}(\omega_2)$ and $V_{IIP3,ov}^2(\omega_1)$ are defined in the standard. On the other hand, $NF_{ov}(\omega_1)$ and $V_{IIP3,ov}^2(\omega_2)$ are estimated based on (2.28) and (2.29), respectively. Also, the above result shows that the overall power consumption has a less dependency on the separation of the two frequency bands

when compared to the case of an LNA with decreasing gain. This result indicate that the gain of the LNA is an important design parameter in MB-SS receivers and it should be considered during the block-level budgeting design phase.

4. Numerical Example for DB-SS Receiver

In this section, a numerical example is demonstrated to clarify the importance of including the gain behavior of the LNA in the block-level budgeting. The following steps are taken to determine the block-level specifications for minimum power consumption assuming an LNA with constant or decreasing gain with frequency:

- Obtain the BER specifications from the wireless standard.
- Determine the necessary SNR_o from system-level simulations or by using (2.1).
- Determine the minimum NF_{ov} and $V_{IIP3,ov}^2$ that satisfies the SNR_o using (2.2) and (2.3).
- Depending on the gain versus frequency behavior, find the required NF_{ov} and $V_{IIP3,ov}^2$ for the two bands. Lower power consumption is achieved if an LNA with constant gain response is used.
- Find the budget of each building block to satisfy the BER of the standard using (2.17) and (2.18).

The above steps are applied for a homodyne dual-band receiver, shown in Fig. 6, for mobile communication standards. The first band is considered as GSM at 900 MHz, while the higher band is considered as PCS at 1900 MHz. In this analysis, recent published receiver specifications with an NF_{ov} lower than 4 dB, and a $V_{IIP3,ov}^2$ higher than -12 dBm using 0.25 μm CMOS technology is assumed. The sensitivity of the receiver is -102 dBm, which means an overall gain of 100 to 107 dB is required.

Table I. Power coefficients of various blocks of the receiver.

$P_{c,LNA}$	$P_{c,Mixer}$	$P_{c,Filter}$
$5.6 \cdot 10^{-20} \text{ [W/Hz]}$	$7.3 \cdot 10^{-18} \text{ [W/Hz]}$	$11.4 \cdot 10^{-18} \text{ [W/Hz]}$

Typical values for the power coefficient, for a 2.8 V supply, of the receiver are assumed. These values are obtained by making a search over the available designs using the $0.25\mu\text{m}$ technology node, and they are tabulated in Table I.

The proposed design methodology is applied for the two gain cases of the LNA to find the block specification. Table II shows the block specifications of the optimized dual-band receiver. As depicted, for the first case (LNA with decreasing gain), the lower band has the worst non-linearity, while the upper band has the worst noise figure. For this case, the NF_{ov} is 1.26 dB for the lower frequency band, while it is 4 dB for the upper band. $V_{IIP3,ov}^2$ is -12 dBm and -5 dBm for the lower and upper bands, respectively.

For the second case with constant gain, the NF_{ov} is 3 dB and 4 dB for the lower and upper bands, respectively. $V_{IIP3,ov}^2$ is -12 dBm and -11.5 dBm for the lower and upper bands, respectively. These results indicate that the overall performance specifications of the receiver at the two different bands is almost similar. It should be mentioned that the first case is hard to realize because it is difficult to implement an LNA with an NF of 0.2 dB at 900 MHz. On the other hand, the second case is simpler to realize.

Table II. Block-level specifications for dual-band GSM/PCS receiver.

	LNA			Mixer		Filter	
	NF	IIP3	A	NF	IIP3	NF	IIP3
	[dB]	[dBm]	[dB]	[dB]	[dBm]	[dB]	[dBm]
Case 1 (ω_1)	0.2*	-3.4	16	8	8	20	19.3
Case 1 (ω_2)	0.82	3	9.6	8	8	20	19.3
Case 2 (ω_1)	0.6	-3.4	16	12.3	8	24.7	19.3
Case 2 (ω_2)	2.12	3	16	12.3	8	24.7	19.3

0.2 dB is not possible to implement using existing technologies.

Finally, the power consumption ratio between the two cases is derived using (2.25) and (2.30) and it is given by

$$\frac{P_{ov,case1}}{P_{ov,case2}} = \left(\frac{\omega_2}{\omega_1}\right)^2 \frac{\sqrt[3]{P_{c,1}}\left(\frac{\omega_1}{\omega_2}\right)^2 + \sum_{j=2}^n \sqrt[3]{P_{c,j}}}{\sum_{j=1}^n \sqrt[3]{P_{c,j}}} = 3.98. \quad (2.31)$$

The above expression indicates that more power is wasted if the ratio $\left(\frac{\omega_2}{\omega_1}\right)$ is increased. Hence, having an LNA with constant gain helps in reducing the overall power consumption of the receiver, which is 75% in this case.

D. Optimum Block-Level Budgeting for MB-MS Receivers

Block-level budgeting of a MB-MS CMOS receiver can be divided into three cases as discussed below: (1) multiple bands with same standard (MB-SS); (2) multiple standards existing at the same frequency band (SB-MS); and (3) combination of the two cases (MB-MS).

1. Case 1: Multiple Bands, Single Standard (MB-SS)

In this case, the same standard covers several frequency bands, as in GSM 900 and 1900 MHz bands. Three possible system-level design approaches can be applied. The first approach uses parallel receiver chains for different frequency bands, where each chain is optimized individually for minimum power consumption as defined in (2.13) and (2.14). Parallel chains increases the area and the cost of the CMOS receiver, but it results in the minimal possible power consumption. The second approach is to assume that the same receiver chain is used for all bands and LNA has a constant gain over the entire band. In this case, the worst NF_{ov} and $V_{IIP3,ov}^2$ among the several standards should be considered leading to a DR_{ov} higher than the required DR_{ov} for each band. The third approach, which is considered in this work, assumes that the same receiver chain is used and the gain of the LNA is variable with the frequency band.

For a MB-SS receiver, the frequency dependency of NF_{ov} and $V_{IIP3,ov}^2$ must be considered during the block-level budgeting for minimum power consumption. Therefore, (2.15) is modified to include the frequency dependency as following

$$P_{ov} = \frac{V_{IIP3,ov}^2(\omega)}{(NF_{ov}(\omega) - 1)kT \cdot 50} \left(\sum_{j=1}^n \sqrt[3]{P_{c,j}} \right)^3, \quad (2.32)$$

where ω is the operating frequency. Commonly NF_{ov} and $V_{IIP3,ov}^2$ change as the operating frequency changes in CMOS receivers. For the receiver chain in Fig. 6, this change is due to the dependency of NF and V_{IIP3}^2 of the LNA to the operating frequency. As a result, NF_{ov} and $V_{IIP3,ov}^2$ should be examined for several bands in MB-SS receivers. For example, if band 1 has lower frequency than band 2, and if NF_{ov} increases with frequency, then NF_{ov} of band 1 should be adjusted to a value lower than the one specified by the standard. Hence, DR_{ov} at band 1 should be higher

than the one specified by the standard. This frequency dependency leads usually to a higher power consumption. Similar conclusion is obtained if $V_{IIP3,ov}^2$ frequency dependency is considered. It is important to minimize DR_{ov} for a given standard as follows

$$DR_{ov,min}(\omega_k) = \frac{V_{IIP3,ov,min}^2(\omega_k)}{(NF_{ov,max}(\omega_k) - 1)KT \cdot 50}, \quad (2.33)$$

where $V_{IIP3,ov,min}^2$ and $NF_{ov,max}$ are specified by the standard, and the subscript k stands for the k^{th} frequency band. To keep P_{ov} minimum over multiple frequency bands, DR_{ov} should be minimized across these bands, i.e $NF_{ov}(\omega_1) = \dots = NF_{ov}(\omega_k) = \dots = NF_{ov}(\omega_N) = NF_{ov,max}$, $V_{IIP3,ov}^2(\omega_1) = \dots = V_{IIP3,ov}^2(\omega_k) = \dots = V_{IIP3,ov}^2(\omega_N) = V_{IIP3,ov,min}^2$. N is the number of frequency bands. Keeping both NF_{ov} and $V_{IIP3,ov}^2$ the same across different frequency bands is not trivial because NF_{ov} is related to the frequency-dependent noise figure of the LNA while $V_{IIP3,ov}^2$ is dependant to the baseband building block of the receiver chain. Therefore, the receiver has different DR_{ov} values at different frequencies. In such a case, either NF_{ov} or $V_{IIP3,ov}^2$ should be kept constant over different frequency bands to minimize DR_{ov} , and hence the power consumption. Assuming NF_{ov} is the same for various bands, the following condition holds using (2.12)

$$\overline{V_{ni,LNA}^2}(\omega_1) + \frac{\overline{V_{ni,2:n}^2}}{A_{LNA}^2(\omega_1)} = \overline{V_{ni,LNA}^2}(\omega_k) + \frac{\overline{V_{ni,2:n}^2}}{A_{LNA}^2(\omega_k)}, \quad (2.34)$$

where the subscript $2 : n$ indicates the effective input referred noise of the CMOS receiver chain excluding LNA. As depicted in (2.34), the gain of the LNA can be adjusted to satisfy the required condition. By solving (2.34) using (2.13) and (2.14), one can prove that there is an optimum gain variation of the LNA at different frequency

bands to provide the same NF_{ov} as follows

$$\frac{A_k^2}{A_1^2}|_{NF,ov} = \frac{1}{1 + \frac{\sqrt[3]{P_{c,LNA}}}{\sum_{j=2}^n \sqrt[3]{P_{c,j}}} \cdot \left(1 - \frac{V_{ni,LNA}^2(\omega_k)}{V_{ni,LNA}^2(\omega_1)}\right)}. \quad (2.35)$$

To calculate the necessary gain ratio, the noise figure or input referred noise ($\overline{V_{ni,LNA}^2}$) variation of the LNA versus frequency is also required. For the same NF_{ov} over different frequency bands, $V_{IIP3,ov}^2(\omega_1)/V_{IIP3,ov}^2(\omega_k)$ ratio is given by

$$\frac{V_{IIP3,ov}^2(\omega_1)}{V_{IIP3,ov}^2(\omega_k)} = \frac{\left(\frac{V_{IIP3,LNA}^2(\omega_1)}{V_{IIP3,LNA}^2(\omega_k)} + \frac{\sum_{j=2}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,LNA}}} \cdot \frac{A_k^2}{A_1^2}|_{NF,ov}\right)}{\sum_{j=1}^n \sqrt[3]{P_{c,j}} / \sqrt[3]{P_{c,LNA}}}. \quad (2.36)$$

Similarly, if $V_{IIP3,ov}^2$ is kept constant over different bands instead of NF_{ov} , the gain variation of the LNA and $NF_{ov}(\omega_1)/NF_{ov}(\omega_k)$ ratio are given by

$$\frac{A_k^2}{A_1^2}|_{V_{IIP3,ov}^2} = 1 + \frac{\sqrt[3]{P_{c,LNA}}}{\sum_{j=2}^n \sqrt[3]{P_{c,j}}} \cdot \left(1 - \frac{V_{IIP3,LNA}^2(\omega_1)}{V_{IIP3,LNA}^2(\omega_k)}\right), \quad (2.37)$$

$$\frac{NF_{ov}(\omega_1) - 1}{NF_{ov}(\omega_k) - 1} = \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}} / \sqrt[3]{P_{c,LNA}}}{\frac{V_{ni,LNA}^2(\omega_k)}{V_{ni,LNA}^2(\omega_1)} + \frac{\sum_{j=2}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,LNA}}} \cdot \frac{A_1^2}{A_k^2}|_{V_{IIP3,ov}^2}}. \quad (2.38)$$

To check the validity of the above equations, the required overall system-level specifications for different frequency bands are simulated versus different gain ratios of the LNA using MATLAB ¹. For each simulation point, the receiver chain is optimized for minimum power consumption using (2.13) and (2.14). Also, NF_{ov} and $V_{IIP3,ov}^2$ at each frequency band are adjusted manually to take into account the frequency dependency of NF_{LNA} and $V_{IIP3,LNA}^2$. The simulation results for 900 and 1900 MHz frequency bands are presented in Fig. 8. The simulated response can be divided into three regions. In region 1, $V_{IIP3,ov}^2(\omega_1)$ and $NF_{ov}(\omega_2)$ are set to -12 dBm and 4 dB,

¹MATLAB v.7.0, MathWorks, Inc.

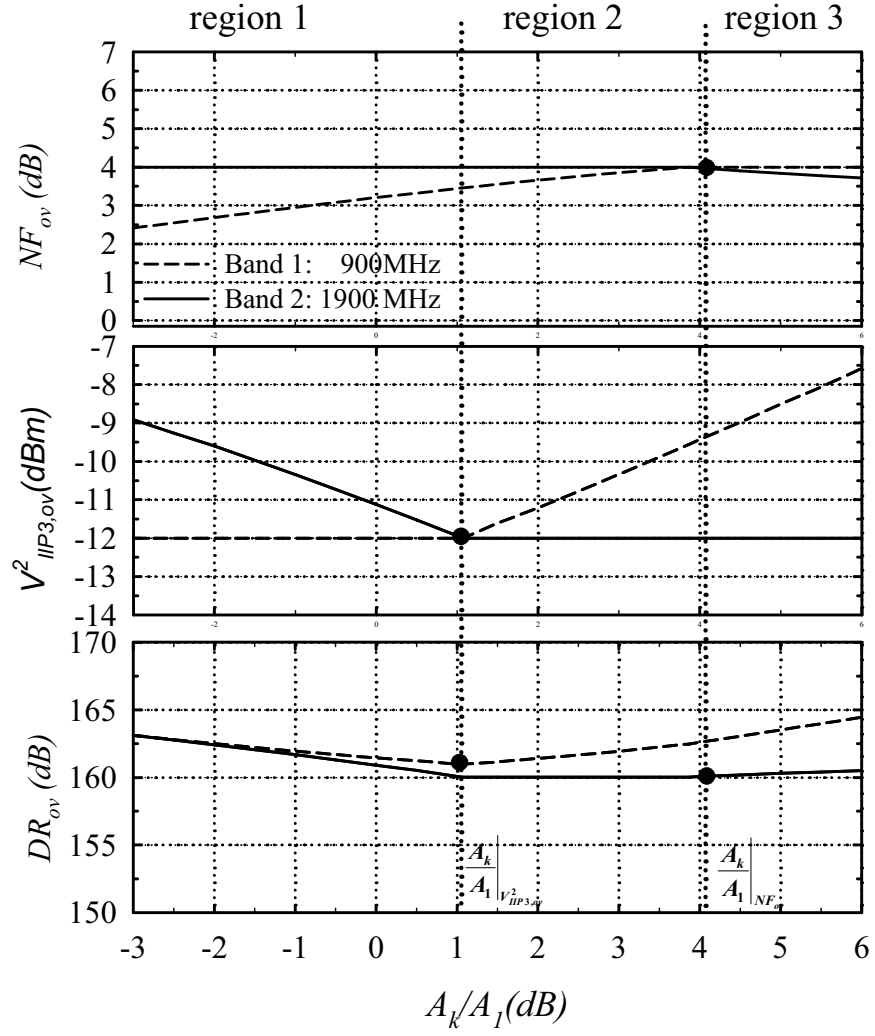


Fig. 8. NF_{ov} , $V^2_{IIP3,ov}$ and DR_{ov} for a dual-band system (Band 1: 900 MHz, Band 2: 1900 MHz, $A_1=16$ dB, $NF_{ov} < 4$ dB, $V^2_{IIP3,ov} > -12$ dBm).

respectively. These values are specified by the standard. As the gain ratio increases, $NF_{ov}(\omega_1)$ increases and $V_{IIP3,ov}^2(\omega_2)$ decreases until one of the two parameter reaches the boundary of region 2. In this example, $V_{IIP3,ov}^2(\omega_2)$ determines the starting point of this region. By increasing the gain ratio, $V_{IIP3,ov}^2(\omega_2)$ reduces to a value lower than the one specified by the standard. For this reason, $V_{IIP3,ov}^2(\omega_2)$ is set to -12 dBm, and hence $V_{IIP3,ov}^2(\omega_1)$ increases with the gain ratio. $NF_{ov}(\omega_1)$ reaches to its maximum allowable value at the beginning of region 3, and therefore $NF_{ov}(\omega_2)$ needs to be reduced if the gain ratio increases beyond this point. This example shows that DR_{ov} has two turning points (defined by (2.35) and (2.37)). DR_{ov} reaches to a minimum value on one of these two points. For this example, minimum DR_{ov} is obtained when $V_{IIP3,ov}^2$ is the same for both bands. Comparing the optimum design point, which requires two gain settings, with the case of constant gain ($\frac{A_k}{A_1} = 0$ dB), the optimum design approach reduces DR_{ov} by 0.5 dB, which is equivalent to reducing P_{ov} by 12%. This simulation example indicates that the gain variation of the LNA is an important parameter to minimize P_{ov} , and an LNA with two gain settings achieves the required target with a gain difference of 1 dB.

For the general case of MB-SS receiver, the required DR_{ov} for each frequency band, ω_k , is calculated using the same methodology with respect to the lowest frequency band (ω_1). The required gain ratio, A_k/A_1 , for different frequency bands is calculated from (2.35)-(2.38). Then, the required $NF_{ov}(\omega_1)$ and $V_{IIP3,ov}^2(\omega_1)$ are determined from the following relations

$$\begin{aligned} V_{IIP3,ov}^2(\omega_1) &= \max \left(V_{IIP3,ov}^2(\omega_1)|_{\omega_2}, \dots, V_{IIP3,ov}^2(\omega_1)|_{\omega_N} \right), \\ NF_{ov}(\omega_1) &= \min \left(NF_{ov}(\omega_1)|_{\omega_2}, \dots, NF_{ov}(\omega_1)|_{\omega_N} \right). \end{aligned} \quad (2.39)$$

where $V_{IIP3,ov}^2(\omega_1)|_{\omega_k}$ and $NF_{ov}(\omega_1)|_{\omega_k}$ are the required overall input referred third order intercept point and noise figure of band k with respect to band 1. Finally, the block-level budgeting is optimized for minimum P_{ov} using (2.13) and (2.14).

2. Case 2: Single Band, Multiple Standards (SB-MS)

The second case assumes the receiver has the same frequency band for several standards such as Bluetooth, WiFi and Zigbee at 2.4 GHz. Similar to case 1, three possible system-level design approaches can be applied to minimize the power consumption. The first approach uses parallel receiver chains for different standards, where each chain is optimized individually for minimum power consumption as defined in (2.13) and (2.14). This approach results in the minimal possible power consumption, however it increases the area and the cost of the CMOS receiver. The second approach is to assume that the same receiver chain with a constant gain LNA is used. In this case, the worst NF_{ov} and $V_{IIP3,ov}^2$ among the several standards should be considered leading to a DR_{ov} higher than the required DR_{ov} for each standard.

The third approach, which is considered in this work, assumes the gain of the LNA is variable with the standard using the same receiver chain. Consider an SB-DS receiver where $NF_{ov,s=1}$ and $NF_{ov,s=2}$ are 3 and 4 dB, and $V_{IIP3,ov,s=1}^2$ and $V_{IIP3,ov,s=2}^2$ are -18 and -12 dBm, respectively. The subscript s stands for the standard. Using the second approach, the receiver has to be optimized for worst NF_{ov} and $V_{IIP3,ov}^2$ of 3 and -12 dBm, respectively. For the third approach, the receiver is optimized for NF_{ov} and $V_{IIP3,ov}^2$ of 4 dB and -12 dBm, respectively. These values are for the standard with maximum DR_{ov} . The overall specification of the other standard is satisfied by lowering the gain of the LNA by 6.5 dB for $s = 2$ when compared to $s = 1$. As a result, $NF_{ov,s=1}$ and $V_{IIP3,ov,s=1}^2$ are 1.8 dB and -18 dBm, respectively. The third approach reduces DR_{ov} and P_{ov} by 1.8 dB (33%) compared to the second approach.

Hence, the block-level budgeting for an SB-MS receiver is performed by finding the required DR_{ov} for all the standard, and selecting $DR_{ov,s=s_{max}}$

$$DR_{ov,s=s_{max}} = \max (DR_{ov,s=1}, \dots, DR_{ov,s=h}, \dots, DR_{ov,s=S}) \quad (2.40)$$

where S is the total number of standards, h is the index for the h^{th} standard, and s_{max} is the standard with maximum DR_{ov} . The block-level specifications are then optimized for the standard with maximum DR ($NF_{ov,s=s_{max}}$ and $V_{IIP3,ov,s=s_{max}}^2$) using (2.13) and (2.14). Because the receiver is designed for $DR_{ov,s=s_{max}}$, any other standard is satisfied by changing the gain of the LNA. If $NF_{ov,s=h}$ is lower than $NF_{ov,s=s_{max}}$, then the gain has to be increased. Using (2.12) the gain ratio of the LNA for the standard h to s_{max} is given by

$$\frac{A_h^2}{A_{s_{max}}^2} \Big|_{NF_{ov}} = \frac{\frac{\sum_{j=2}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,LNA}}}}{\frac{NF_{ov,s=h}-1}{NF_{ov,s=s_{max}}-1} \cdot \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,LNA}}} - 1}. \quad (2.41)$$

On the other hand, if $V_{IIP3,ov,s=h}^2$ is higher than $V_{IIP3,ov,s=s_{max}}^2$, then gain of the LNA has to be decreased. In this case, the gain ratio is

$$\frac{A_h^2}{A_{s_{max}}^2} \Big|_{V_{IIP3,ov}^2} = \frac{\frac{V_{IIP3,ov,s=s_{max}}^2}{V_{IIP3,ov,s=h}^2} \cdot \frac{\sum_{j=1}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,LNA}}} - 1}{\frac{\sum_{j=2}^n \sqrt[3]{P_{c,j}}}{\sqrt[3]{P_{c,LNA}}}}. \quad (2.42)$$

3. Case 3: Multiple Bands, Multiple Standards (MB-MS)

This case is considered a superposition of the two cases discussed previously with S standards occupying N frequency bands. The block-level budgeting for the MB-MS case is obtained in three steps: Step 1) mapping specifications for all standards into the lowest band, Step 2) maximum dynamic range estimation/block-level budgeting considering all standards in the lowest band, and Step 3) mapping all the standards

back to their original frequency band. The first step maps all the standards occupying different bands to the lowest frequency band using (2.35)-(2.38). This step converts the MB-MS case to an SB-MS one, and allows the designer to make an accurate comparison among the required DR_{ov} s of different standards, since all of them are in the same band. The frequency-dependent gain variations for LNA, A_k/A_1 , are also known from Step 1.

The second step solves an SB-MS problem using (2.40)-(2.42). The maximum DR_{ov} is initially determined and then the block-level budgeting for $DR_{ov,s=s_{max}}$ is performed. Finding the standard-dependent gain variations for LNA, $A_h/A_{s_{max}}$, is also a part of this step. The final step, maps back standards to their original operating bands by adjusting the frequency-dependent gain variations of the LNA. The total gain variation for different standards is finally found from

$$\frac{A_{t_{h,k}}^2}{A_1^2} = \frac{A_h^2}{A_{s_{max}}^2} \cdot \frac{A_k^2}{A_1^2}. \quad (2.43)$$

where $A_{t_{h,k}}$ is total gain of the h^{th} standard at k^{th} band.

4. Case Study and Verification

The described system-level design methodology for MB-MS receivers is investigated for a multi-mode CMOS receiver architecture shown in Fig. 6. In this design example, GSM bands at 900 and 1900 MHz, GPS L1 band at 1.575 GHz, and WCDMA at 2.1 GHz are considered. The targeted specifications for each standard are summarized in Table III. Such a receiver can be found in [35]. The NF_{LNA} and $V_{IIP3,LNA}^2$ are assumed to vary with the square root of the frequency as in [36]. Power coefficients of building blocks can be obtained from typical values of their NF , $IIP3$ and power consumption. These values are shown in Table IV.

The results of the design methodology is tabulated in Table IV. NF and $IIP3$

Table III. Targeted system-level requirements.

	GSM-900	GSM-1900	GPS	WCDMA
Band (MHz)	900	1900	1575	2100
NF (dB)	4	4	3	7.9
IIP3 (dBm)	-12	-12	-25	-18
Gain (dB)	104	104	75	70

of the LNA, mixer and baseband blocks are determined mainly from the GSM standard at 1900 MHz, because it has the maximum dynamic range compared to other standards when they are all mapped to the lowest frequency band. $NF_{ov}(\omega_1)|_{\omega_2}$ is 3.8 dB in this case. NF_{LNA} and $V_{IIP3,LNA}^2$ change for different frequency bands due to their frequency dependency. For the mixer and baseband blocks, performance parameters are similar for all standards. $V_{IIP3,ov}^2$ of GPS and WCDMA are higher than the one specified by the standard because the linearity of the receiver is limited by the GSM band. Increasing the gain ratio for these two standards results in a better NF_{ov} and lower $V_{IIP3,ov}^2$. For example for WCDMA case, the gain of the LNA can be increased up to 23.5 dB, where $V_{IIP3,ov}^2$ reaches to -18 dBm. This shows that the gain for WCDMA can be adjusted between 10.5 and 23.5 dB, without changing P_{ov} . In summary, an LNA with four gain settings (10.5, 16, 16.7, 20.3), defined in Table IV, minimizes P_{ov} .

To check the validity of the presented design methodology, the design space of the complete receiver is explored with two billion samples using MATLAB. Each sample contains NF , V_{IIP3}^2 , and gain of each building block. Only forty million samples met all standards. Fig. 9 shows the number of samples versus the estimated P_{ov} normalized

Table IV. Block-level specifications for MB-MS CMOS receiver (NF and $Gain$ in dB, v_n in $\frac{nV}{\sqrt{Hz}}$, and $IIP3$ in dBm, $P_{c,LNA} = P_{c,BB} = 1.1 \cdot 10^{-17}W$, $P_{c,Mixer} = 7.3 \cdot 10^{-18}W$).

		GSM-900		GSM-1900		GPS		WCDMA	
Case ¹		C1	C2	C1	C2	C1	C2	C1	C2
LNA	NF	1.74	1.18	2.34	1.63	2.18	1.5	2.44	1.7
	$IIP3$	-7.4	-7.4	-5.3	-5.7	-6.2	-6.18	-5.6	-5.56
	$Gain$	16	16	16.7	16	20.3	16	10.5	16
Mixer	v_n	1.88	1.5	1.88	1.5	1.88	1.5	1.88	1.5
	$IIP3$	9.2	9.2	9.2	9.2	9.2	9.2	9.2	9.2
	$Gain$	12	12	12	12	12	12	12	12
BB	v_n	8.06	6.4	8.06	6.4	8.06	6.4	8.06	6.4
	$IIP3$	20.5	20.5	20.5	20.5	20.5	20.5	20.5	20.5
	$Gain$	76	75	75.3	76	42.7	47	47.5	42
Total	NF	3.84	2.8	4	3.1	3	3	7	3.2
	$IIP3$	-12	-12	-12	-11.5	-15	-11.6	-8.1	-11.4

¹C1: proposed methodology C2: fixed gain LNA

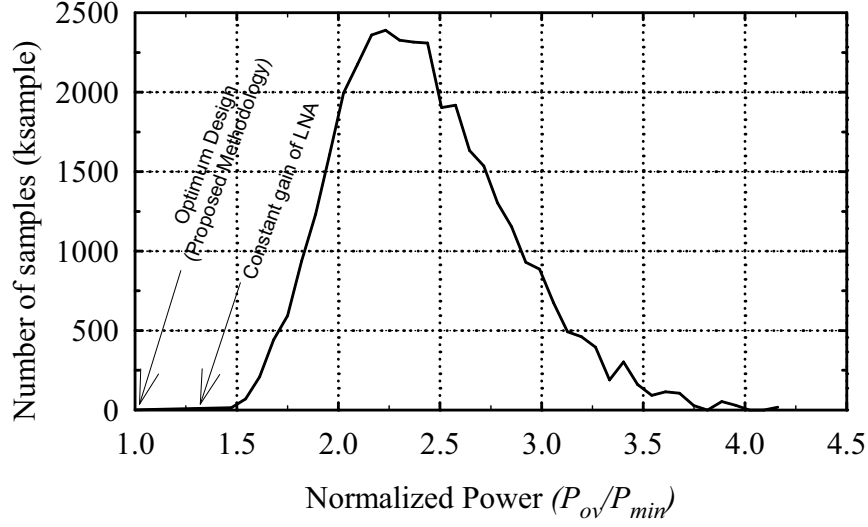


Fig. 9. Number of samples versus the normalized power (P_{ov}/P_{min}) for different block-level specifications of the multi-mode receiver.

to power consumption obtained using the proposed system-level design methodology. The power consumption for all design points are calculated from $\sum_{j=1}^n P_{c,i} \cdot DR_i$. None of simulated design points resulted in P_{ov} lower than the one obtained using the proposed methodology, hence showing that the proposed methodology is the optimum one. Also, as the ratio P_{ov}/P_{min} is minimized, the number of samples is decreased exponentially, which shows the difficulty to find the optimum design point using manual approaches.

The proposed methodology is compared to the case where a fixed gain wideband LNA is used as in [37]. In addition, the comparison with the case of the LNA with constant gain is just to clarify the importance of having an LNA with different gain settings for the various bands and standards to minimize the power consumption. The result is tabulated in Table II. For fixed gain LNA case, a minimum NF_{ov} and $V_{IIP3,ov}^2$ of 2.8 dB and -12 dBm at 900 MHz is obtained, respectively. The resulted

DR_{ov} is higher by 2.1 dB when compared to the optimum case resulting in a higher power consumption. Using $\sum_{j=1}^n P_{c,i} \cdot DR_i$ to compute the estimated power consumption in each case, the presented design methodology shows a reduction in the power consumption by 40% when compared to the case of wideband LNA with fixed gain.

E. Summary

A MB-MS receiver was considered as superposition of a MB-SS and SB-MS receiver. Analytical expressions for NF and V_{IIP3}^2 of each building block were provided to minimize the overall power consumption. The gain variation of the LNA for different standards/bands is an important factor which determines the power consumption. The methodology was tested for a wideband receiver covering GSM-900, GSM-1900, GPS and WCDMA standards. As an example, the power consumption is reduced by 40% when compared to the approach where the gain of the LNA is kept constant.

CHAPTER III

24/31 GHZ DUAL-BAND SWITCHABLE HARMONIC RECEIVER

The growing number of wireless applications in the communication market is one of the main drivers of the semiconductor industry. With the increasing demand for high data rate communication, and the congestion of the low-gigahertz frequency bands, moving to the largely unused spectrum at millimeter-wave (mm-wave) frequencies is necessary. Some system applications include IEEE 802.16 wireless metropolitan area network (WiMAN) for point-point wireless communications at 10-66 GHz frequency range, automotive short-range and long-range radars for collision avoidance at 22-29 and 77 GHz, and cognitive radios. Several CMOS/BiCMOS based single-band silicon-based transceivers are reported for mm-wave applications [2, 4, 5, 6, 38]. The idea of combining multiple bands is also very appealing for mm-wave transceivers on silicon to increase the versatility and save the chip area.

Single-band receivers at millimeter-wave frequencies have been the main focus of many literatures till now. The first 24 GHz CMOS front-end in a 0.18- μm process was reported in [2]. A receiver front-end that incorporated folded microstrip geometry to create resonance at 60 GHz band in a common-gate low noise amplifier and active quadrature mixers was realized in 0.13- μm CMOS technology [38]. Guan et al. [4] reported a fully-integrated 8-channel phased-array heterodyne receiver at 24 GHz ISM (Industrial, Scientific, Medical) band in BiCMOS technology. Receiver chipsets for gigabit per second wireless communications in the 60 GHz ISM band in BiCOMS and CMOS technologies were demonstrated in [5, 8, 39]. A fully-integrated phased array receiver with integrated dipole antennas for long-range automotive radar applications at 77 GHz was designed and fabricated in a 0.12- μm BiCMOS process in [6]. As can be seen, most of the efforts have been concentrated on developing the first generation

of single-band commercial silicon receivers at 24, 60 and 77 GHz.

Implementing dual/multi-band receivers on silicon poses many challenging problems at mm-wave frequencies as follows: 1) frequency synthesizers need to span over a very wide frequency range to cover the entire band of interest. As a result, they are power hungry or very hard to implement due to the wide tuning range of voltage controlled oscillator (VCO), and 2) front-end building blocks including LNA and mm-wave mixer have to support very wide frequency range. Hence, receiver architectures which rely on frequency synthesizers running at lower frequencies, and new front-end topologies which support multi-gigahertz frequency range need to be developed to overcome the above challenges.

The first dual-band 22-29/77-81 GHz transceiver for automotive radars have been recently reported using BiCMOS technology [11]. The transceiver is based on a direct conversion receiver architecture along with a dual-band low noise amplifier and frequency synthesizer. To avoid having a very wide tuning range of the VCO, this receiver architecture uses two local oscillators for each separate band. In addition, these local oscillators have to run at 22 and 77 GHz, which result in high power consumption. This receiver shows that direct conversion receivers are not suitable for multi-band operation at mm-wave frequencies because of the limited tuning range of the local oscillator. To the best of our knowledge, there is no other reported dual/multi-band silicon-based radio at mm-wave frequencies.

In this chapter, a new dual-band architecture is proposed to down-convert the ISM and LMDS (Local Multipoint Distribution Service) bands at 24 and 31 GHz, respectively. The receiver is targeted for the single carrier wireless metropolitan area network standard (IEEE 802.16). Table V summarizes the key specifications of this standard. For the designed receiver, it is assumed that the receiver is a QPSK modulator and it should achieve a BER of 10^{-3} . Our system level simulations show

Table V. Summary of the IEEE802.16 standard.

Parameter	Value	Parameter	Value
Frequency Range	10-66 GHz	MDS	-30 dBm
Channel Spacing	20/25/28 MHz	Modulation	QPSK, 16-QAM, 64-QAM
Sensitivity	-81 dBm BER 10^{-3} -77 dBm BER 10^{-6}	Max. Bit rate	134 Mbit/s

that the required overall noise figure is around 12 dB and the total input referred third order intercept point, $IIP3$, of the system should be higher than -24 dBm to achieve the specified BER. These values agree with values defined in the standard's documentation [1].

The proposed receiver relies on a switchable harmonic mixer for band selection. The switchable harmonic mixer allows the local oscillator to run at a lower frequency, hence eliminating the need for a wide band VCO (challenge 1). In addition, new circuit techniques for a wideband low noise amplifier and wideband mm-mixer are employed to cover the frequency band of interest and to further reduce the power consumption (challenge 2). The chapter is organized as follows: In Section A, the proposed switchable harmonic receiver architecture is presented. Different building blocks of the receiver, including the wide-band low noise amplifier, the wideband mm-mixer and the switchable harmonic mixer, and their implementation are discussed in Sections B-D. Finally, the measurement results are then shown in Section E.

A. Proposed Receiver Architecture

1. Basic Idea

The proposed receiver architecture and its frequency planning are demonstrated in Fig. 10 and Fig. 11, respectively. Similar to the heterodyne receiver, the desired band is down-converted to baseband through an intermediate frequency (f_{IF}). The two frequency bands, at 24 and 31 GHz, are initially amplified using a two-stage wideband low noise amplifier (LNA). Then, a wideband mm-mixer and a local oscillator (LO1) running at $f_{LO1}=10.25$ GHz (effective mixing frequency is 20.5 GHz) is used to down-convert the 24 and 31 GHz bands to intermediate frequencies of 3.5 and 10.5 GHz, respectively. The second mixing stage depends on a switchable harmonic mixer (SWHM) for band selection and final down-conversion of signals to baseband. The second local oscillator (LO2) operates at a frequency of $f_{LO2}=3.5$ GHz and the band selection is achieved by either mixing the input signal with fundamental or third order harmonic component of LO2. The IF amplifier is used to filter out the higher unwanted frequency components, drive the high input capacitance of the switchable harmonic mixer, and provide higher gain at the upper band to compensate the 9 dB systematic gain difference between the lower and upper bands as discussed later in this section.

The basic idea of the band selection is to adjust the harmonics of the second mixing stage. If the 24 GHz is desired, the second mixing stage mixes the input signal with the 3.5 GHz fundamental component, and the third order harmonic component at 10.5 GHz is suppressed. On the other hand, if the 31 GHz band is desired, the fundamental component of the second oscillator is suppressed and the third harmonic component, at 10.5 GHz, is amplified. The mathematical formulation for this operation is discussed later in this section. Because the architecture is based on an

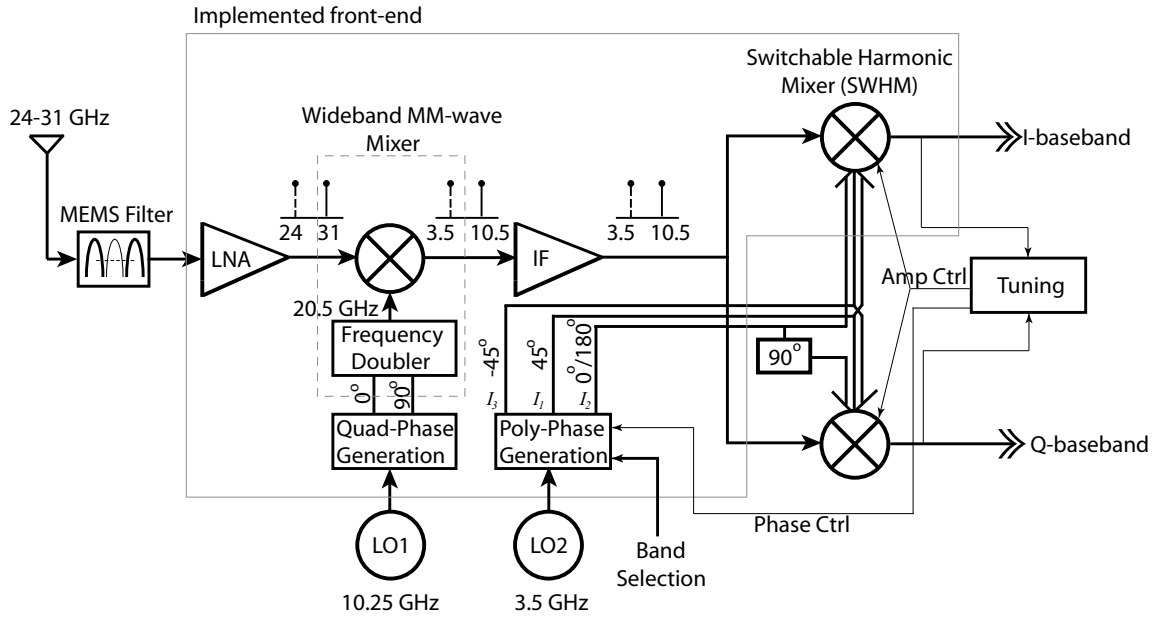


Fig. 10. Proposed switchable harmonic receiver architecture.

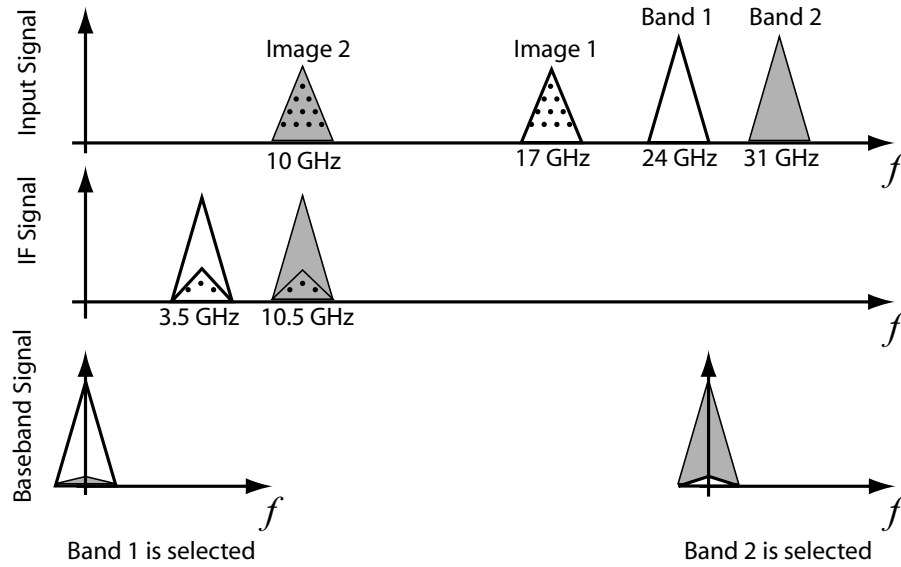


Fig. 11. Frequency planning of the proposed switchable harmonic receiver.

heterodyne scheme, the LNA should provide image rejection to achieve a high signal-to-noise ratio (SNR) from the received data. If the image rejection provided by the LNA is not sufficient for the necessary rejection, an external bandpass filter (such as a switchable RF MEMS filter at 24-31 GHz similar to the one reported in [40]) can be added in front of the receiver to remove unwanted image signals that are placed at 17 and 10 GHz for the 24 and 31 GHz frequency bands, respectively.

To demonstrate the advantage of the proposed receiver architecture, it is compared to one of the existing Weaver-based dual-band receivers [41]. The Weaver based architecture requires a local oscillator that is running at 27.5 GHz compared to one running at 20.5 GHz in the proposed architecture. Having a lower oscillating frequency reduces the power consumption while achieving a better phase noise. For the second mixing stage, both architectures are using the same LO frequency. Another advantage is that the weaver architecture requires two mixers that are operating at 27 GHz compared to a single mixer that is operating at 20.5 GHz. Reducing the number of components at the beginning of the front-end, reduces the power consumption as well as the complexity in the layout due to the coupling among various components. It is important to mention that both architectures require a tuning scheme, such as least mean square (LMS), to efficiently reject one of the bands and receive the desired one [41]. In this implementation, two control lines are used for external tuning. The first adjusts the phase error, while the other one adjusts the gain error.

2. Switchable Harmonic Mixer Mathematical Analysis

The switchable mixer mixes the input signal at 3.5 or 10.5 GHz with either f_{LO2} or $3 \cdot f_{LO2}$, respectively. Fig. 12 demonstrates the idea of the switchable mixer, where a single local oscillator source with three different phases is required to mix the input signal with the fundamental or the third order harmonic, and suppress the

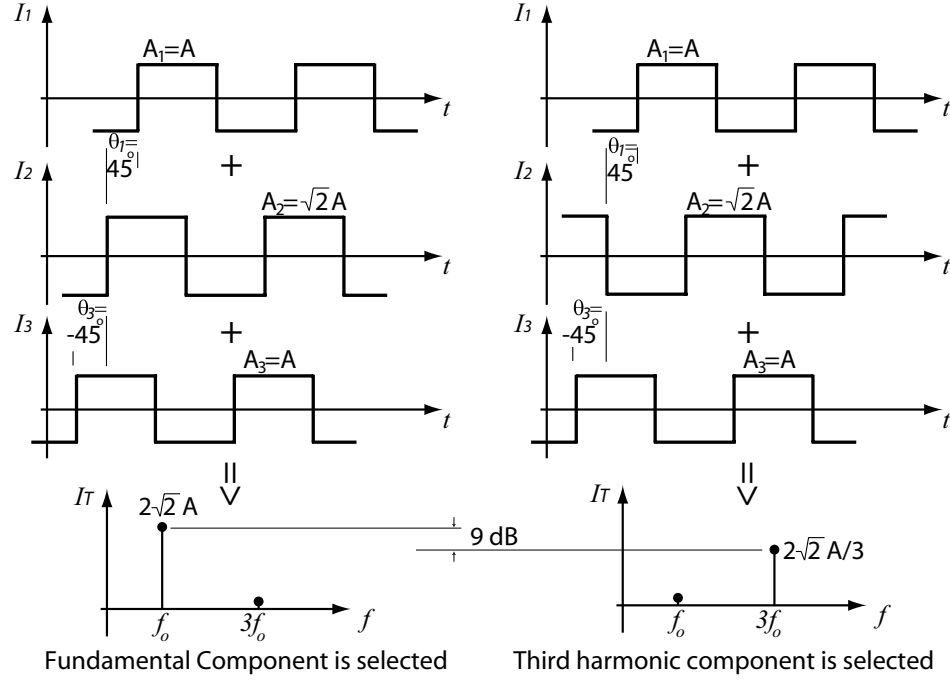


Fig. 12. Basic idea of switchable harmonic mixer.

other components. The three wave forms are considered square waves because this is the effective signal seen by any Gilbert-cell-based mixer. The fundamental or third harmonic components cancellation is achieved by summing the three local oscillator signals, $I_1 - I_3$, with the proper phase and amplitude scaling.

Using Fourier series analysis, the three waveforms are written in terms of their first five harmonics as follows

$$\begin{aligned}
 I_1 &= A_1 \cdot [\cos(\omega t + \theta_1) - \frac{1}{3} \cos(3\omega t + 3\theta_1) + \frac{1}{5} \cos(5\omega t + 5\theta_1)], \\
 I_2 &= A_2 \cdot [\cos(\omega t) - \frac{1}{3} \cos(3\omega t) + \frac{1}{5} \cos(5\omega t)], \\
 I_3 &= A_3 \cdot [\cos(\omega t + \theta_3) - \frac{1}{3} \cos(3\omega t + 3\theta_3) + \frac{1}{5} \cos(5\omega t + 5\theta_3)].
 \end{aligned} \tag{3.1}$$

where A_1 , A_2 , and A_3 are the amplitudes of the three different waveforms, and θ_1

and θ_3 are phase shifts. In these equations, I_2 is selected as the reference signal and therefore $\theta_2 = 0$. The effective mixing signal, I_T , is generated by summing the three waveforms as follows

$$I_T = I_1 + I_2 + I_3. \quad (3.2)$$

With assumptions of $\theta_1 = -\theta_3$ and $A_1 = A_3$, the effective mixing signal can be written as follows

$$\begin{aligned} I_T &= (2 \cdot A_1 \cos(\theta_1) + A_2) \cdot \cos(\omega t) \\ &- \frac{1}{3} \cdot (2 \cdot A_1 \cos(3\theta_1) + A_2) \cdot \cos(3\omega t) \\ &+ \frac{1}{5} \cdot (2 \cdot A_1 \cos(5\theta_1) + A_2) \cdot \cos(5\omega t). \end{aligned} \quad (3.3)$$

The fundamental or the third harmonic component in (3.3) are eliminated by adjusting values of amplitudes and phases of three waveforms I_1 - I_3 . Several amplitudes and phases can perform this functionality, and Fig. 13 shows the required amplitude ratio, A_2/A_1 , for each value of θ_1 to cancel either the fundamental or the third harmonic component. Among these solutions, three practical sets are selected. Table VI summarizes coefficients and component values for these sets.

For the proposed receiver, the first set ($\theta_1 = -\theta_3 = 45^\circ$) is selected because it reduces the hardware complexity. For this set, only the phase of I_2 controls the band selection by changing its polarity. The lower frequency band is selected by tuning the switchable harmonic mixer for $A_1 = A_3 = A_2/\sqrt{2}$, and the upper frequency band is selected by adjusting the mixer to $A_1 = A_3 = -A_2/\sqrt{2}$. On the other hand, Sets 2 and 3 require both polarity and amplitude change of A_2 to perform the band selection. Employing Set 2 or 3 enforces additional complexity in the implementation.

Table VI. Coefficients values of the switchable harmonic mixer for two possible combinations ($A_1 = A_3$).

	Set 1		Set 2		Set 3	
Coefficients	$A_1 = -A_2/\sqrt{2}$ $\theta_1 = -\theta_3 = 45^\circ$	$A_1 = A_2/\sqrt{2}$ $\theta_1 = -\theta_3 = 45^\circ$	$A_1 = -A_2$ $\theta_1 = -\theta_3 = 60^\circ$	$A_1 = A_2/2$ $\theta_1 = -\theta_3 = 60^\circ$	$A_1 = -A_2/\sqrt{3}$ $\theta_1 = -\theta_3 = 30^\circ$	$A_1, A_2 = 0$ $\theta_1 = -\theta_3 = 30^\circ$
f_o component	0	$2\sqrt{2} \cdot A_1$	0	$3 \cdot A_1$	0	$\sqrt{3} \cdot A_1$
$3f_o$ component	$2\sqrt{2}/3 \cdot A_1$	0	$2 \cdot A_1$	0	$1/\sqrt{3} \cdot A_1$	0
$5f_o$ component	$2\sqrt{2}/5 \cdot A_1$	0	0	$3/5 \cdot A_1$	$2\sqrt{3}/5 \cdot A_1$	$\sqrt{3}/5 \cdot A_1$

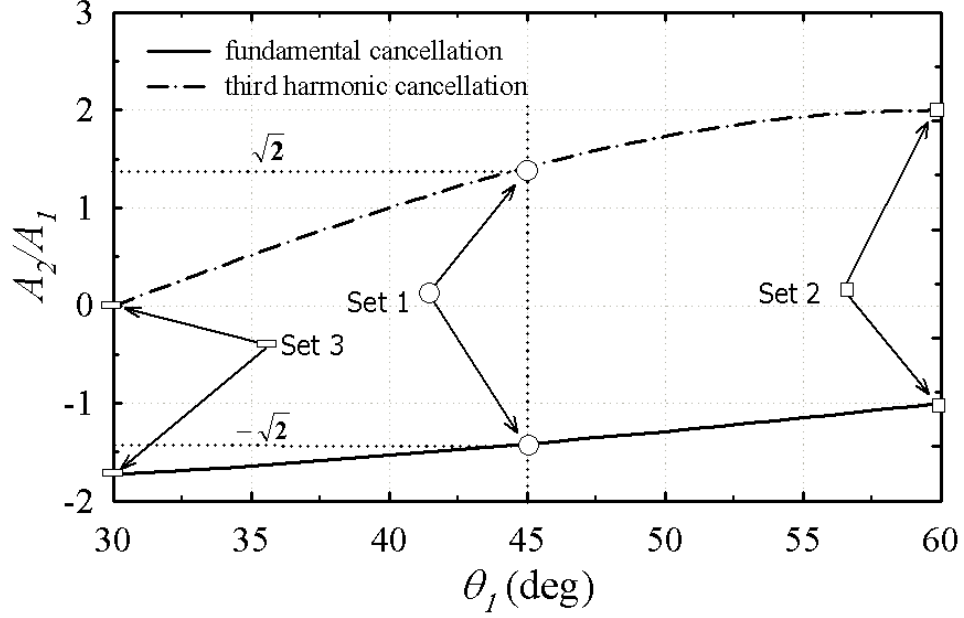


Fig. 13. Phase and Amplitude conditions for fundamental or third harmonic component cancellation.

Another advantage of selecting the 45° phase shift appears when considering Q-mixer implementation in Fig. 10. Only an additional 90° phase shift is required for I_2 LO signal. For the I_1 and I_3 signals, the 90° is inherently generated. This is because shifting I_1 (I_3) by 90° gives the inverted signal of I_3 (I_1), which is already used to drive the I-mixer. This is not the case for Sets 2 and 3, and therefore the 45° phase shift relaxes the receiver complexity.

Table VI also shows the conversion gain of the mixer for each frequency component. For Set 1, there is a systematic gain difference of 9 dB between the fundamental and the third harmonic component. This systematic gain difference is adjusted using the IF amplifier, to provide a flat gain for both frequency bands. Having an almost constant gain for both bands reduces the overall power consumption by relaxing the noise figure and linearity requirements of the following blocks [20]. This idea is veri-

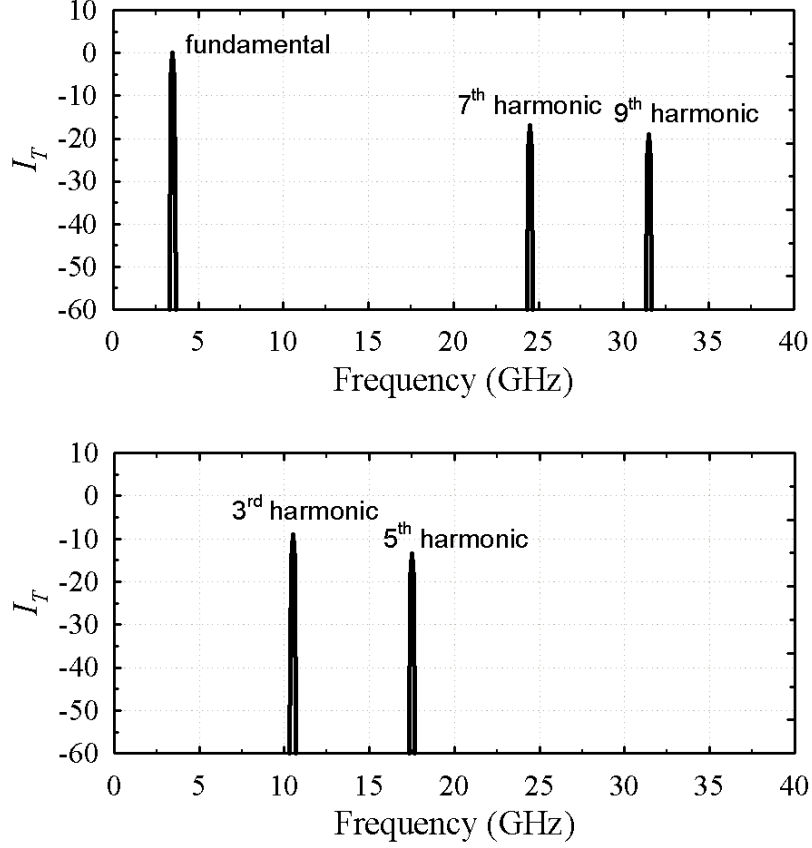


Fig. 14. Simulated spectrum of I_T using Simulink when third harmonic component (top) or fundamental component (bottom) is cancelled using the information of Set 1 in Table VI.

fied using SIMULINK¹ simulations and results are shown in Fig. 14. As depicted, the third and fundamental components are suppressed by adjusting the proper values of the coefficients. Higher order harmonics are easily filtered out using a low-pass filter in the baseband section. The proposed switchable harmonic receiver is not limited to the fundamental or the third order harmonic components, and can be applied to higher order harmonics.

¹SIMULINK: www.mathworks.com

3. Frequency Planning

The proposed dual-band switchable harmonic receiver architecture can be employed to down-convert any arbitrary pair of frequency bands by properly selecting the frequencies of the local oscillators. A general approach to determine the operating frequencies of the two local oscillators is derived as follows

$$f_{LO1} = \frac{3 \cdot f_{band1} - f_{band2}}{2}, \quad f_{LO2} = \frac{f_{band2} - f_{band1}}{2}, \quad (3.4)$$

where f_{LO1} and f_{LO2} are frequencies of local oscillator shown in Fig. 10, and f_{band1} and f_{band2} are the lower and upper frequencies of the two desired bands. For the 24 and 31 GHz bands, f_{LO1} and f_{LO2} are 20.5 and 3.5 GHz, respectively. In this architecture, f_{LO1} is further reduced by using a frequency doubler. As another example for the WiFi standards at 2.4 and 5.2 GHz, $f_{LO1} = 3.8$ GHz and $f_{LO2} = 1.4$ GHz.

4. Sensitivity to Parameter Mismatch

The amount of rejection of the undesired band depends on the matching between various parameters in Table VI. In the following part, a mismatch analysis is performed to investigate the effect of process variations on the amount of rejection, and show the importance of having an automatic tuning scheme for this architecture. Both amplitude and phase mismatches are considered. The amount of rejection, R , is defined as ratio of the received band located at unwanted band, to the desired one. Assuming that the band, existing at the third harmonic component, is rejected, the unwanted component, $I_{T,(3\omega)}$, is as follows

$$\begin{aligned} I_{T,(3\omega)} &= \frac{A_1}{3} \cos(3\omega t + 3\theta_1) + \frac{(A_2 + \Delta A_2)}{3} \cos(3\omega t + 3\Delta\theta_2) \\ &+ \frac{(A_3 + \Delta A_3)}{3} \cos(3\omega t + 3\theta_3 + 3\Delta\theta_3), \end{aligned} \quad (3.5)$$

where ΔA_2 and ΔA_3 are amplitude mismatches, and $\Delta\theta_2$ and $\Delta\theta_3$ are phase mismatches of I_2 and I_3 . In (3.5), the component of A_1 is selected as the reference, and mismatch variations are assumed to happen to the components of A_2 and A_3 . In the ideal case of infinite rejection, $I_{T,(3\omega)}$ is zero, and this is achieved if $A_1 = A_3$, $\theta_1 = -\theta_3$, $\Delta\theta_2 = \Delta\theta_3 = 0$, and $\Delta A_2 = \Delta A_3 = 0$. Applying this condition to (3.5) and after some mathematical simplifications, $I_{T,(3\omega)}$ is approximated as follows

$$\begin{aligned} I_{T,(3\omega)} &= a \cdot \cos(3\omega t) - b \cdot \sin(3\omega t), \\ a &= \frac{[\Delta A_2 - 3A_1\Delta\theta_3 \sin(\theta_3) + \Delta A_3 \cos(\theta_3)]}{3}, \\ b &= \frac{[3A_2\Delta\theta_2 + 3A_1\Delta\theta_3 \cos(\theta_3) - \Delta A_3 \sin(\theta_3)]}{3}. \end{aligned} \quad (3.6)$$

The total power of $I_{T,(3\omega)}$ is obtained by summing the square value of coefficients of sine and cosine functions as follows

$$|I_{T,(3\omega)}| = \sqrt{a^2 + b^2}. \quad (3.7)$$

Finally, the rejection ratio, $R_{1,3}$ of the band, located at third harmonic component, to the fundamental one is given by

$$R_{1,3} = 20 \log \left(\frac{\sqrt{a^2 + b^2}}{|I_{T,(\omega)}|} \right). \quad (3.8)$$

where $I_{T,(\omega)}$ is the amplitude of the fundamental component. Similar analysis can be performed for the case of fundamental component cancelation. Equations (3.6)-(3.8) indicate that the amount of the rejection is a function of amplitudes and phases of the original waveform. Also, these mismatches can add together to worsen the amount of rejection. Fig. 15 shows the worst case rejection versus the value of θ_1 for both $R_{1,3}$ and $R_{3,1}$. The worst case rejection is when all mismatches are added coherently. In this simulation, an amplitude mismatch of $\pm 2\%$ for ΔA_2 and ΔA_3 , and a phase

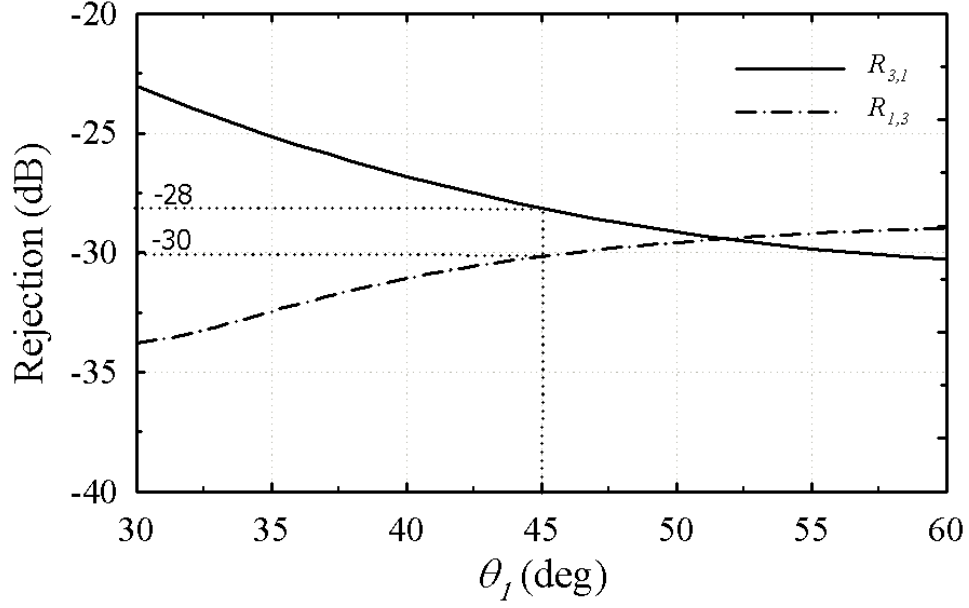


Fig. 15. Worst case rejection for an amplitude and phase mismatches of 2% and 2° , respectively.

mismatch of ± 2 degrees for $\Delta\theta_2$ and $\Delta\theta_3$ are considered. Simulations in Fig. 15 indicate that the worst case rejection depends on the selected value of amplitudes and phases. The lowest value of $R_{1,3}$ is for $\theta_1 = 30^\circ$, while the lowest value of $R_{3,1}$ is for $\theta_1 = 60^\circ$. In this implementation, θ_1 is selected to be 45° because it reduces the receiver complexity as mentioned earlier. The worst case rejection in this case is higher than 28 dB. Using phase and amplitude tuning schemes increases the amount of rejection to values higher than 55 dB similar to the tuning scheme used in the Weaver architecture [41]. Additionally, the external 24-31 GHz RF MEMS switchable bandpass filter provides part of the rejection. Combining both rejection values results in a high rejection that is sufficient to obtain the required high signal to noise ratio.

B. 22-31 GHz Wideband LNA

Wideband low noise amplifiers (LNAs) using silicon were implemented for low-GHz frequencies [42]. For frequencies above 20 GHz (for example K-band within 20-40 GHz), the parasitics limit the wideband operation and increase the overall noise figure of the LNA. In addition, the low cut-off frequency (f_T) of the active devices on silicon limits the upper operating frequency. Also, passive components and interconnections between various devices and building blocks must be individually modeled using electromagnetic simulators to take into account all parasitic effects and achieve the targeted specification after fabrication. All of the above limitations make the design of a wideband LNA within K-band challenging; especially using silicon-based technologies with lower f_T , and hence higher power consumption is a necessity.

Several silicon-based narrowband LNA architectures have been shown in the literature within K-band [2, 43, 44, 45, 46, 47, 48, 49, 50]. A common-gate LNA, operating at 24 GHz, with resistive feedthrough is proposed using 0.18 μm CMOS technology in [2]. This architecture utilizes an inductor and resistor between the drain and source of the input device to reduce the effect of parasitics and noise figure of the common gate topology. The inductor makes this topology narrowband and a 6 dB noise figure is obtained. Utilizing spiral or transmission line-based inductors for the commonly used narrowband inductively degenerated cascode LNA is another approach implemented in [43, 44, 45]. All the techniques in [2, 43, 44, 45] rely on resonance-based loads for narrow-band operation, which is not suitable for the targeted wideband operation. Another narrow-band technique is to utilize stub matching using transmission lines for input and output matching [46]. Stub matching technique also consumes larger area compared to lumped element matching. As can be seen, most of the presented techniques on silicon are suitable for narrowband

operation within K-band.

A wideband LNA for the frequency range of 18-26 GHz was reported using 0.13 μm CMOS technology in [47]. The wideband operation is achieved by utilizing a wideband input matching circuit. Wideband interstage matching was also used to provide the wideband load. Extending this approach to higher frequencies using the same technology may not be suitable because the parasitic capacitance of the second stage has to be decreased which results in reducing the overall gain. The same technique is applied using an advanced 0.13 μm SiGe:C HBT BiCMOS technology to increase the operating frequency and bandwidth [48]. Recently, a wideband LNA for 21-27 GHz using 0.18 μm CMOS technology was reported in [49]. The wideband response is achieved using inductive peaking techniques in the load to extend the bandwidth. For higher bandwidths, the value of the load resistance has to be decreased, and the gain is lowered. For higher gain and bandwidth, the number of stages and the power consumption have to be increased. Employing a third-order Cauer BPF for input matching along with shunt peaking as the load is another technique introduced in [50]. This technique demonstrates a gain of 18 dB for 22-29 GHz operating bandwidth. This survey shows that there is a tradeoff between the bandwidth (BW), gain (G) and power consumption (P) of the amplifier.

In this section, a wideband LNA with coupled-resonators as wideband loads is presented for 23-32 GHz frequency range using 0.18 μm SiGe BiCMOS technology. The proposed approach enables increasing the gain and bandwidth of the amplifier compared to the ones reported in [47, 48, 49, 50], while minimizing the power consumption (higher $G \cdot BW/P$). In addition, a noise reduction technique is employed for the LNA cascode transistor at the first stage to reduce the overall noise figure by resonating out the effect of the parasitic capacitance at the source of the cascode transistor for a wide frequency range. This LNA is targeted for the proposed 24/31

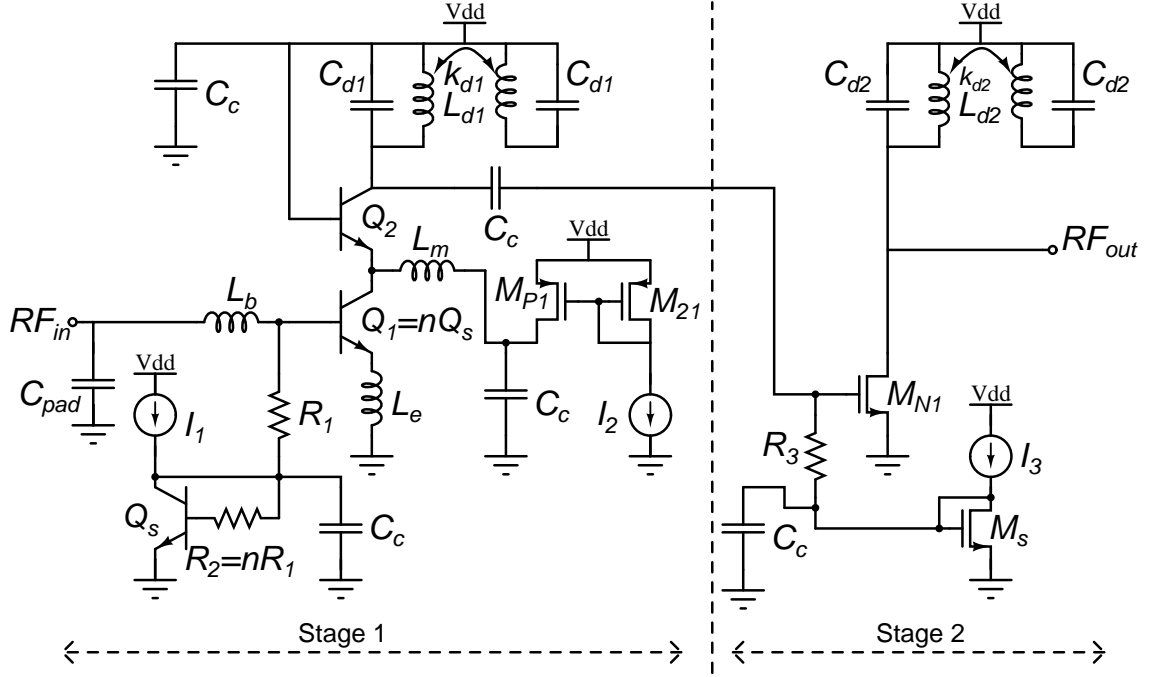


Fig. 16. The schematic of the proposed wideband mm-wave LNA.

GHz dual-band mm-wave receiver. However, it can be used for 22-29 GHz UWB short-range radars.

1. The Proposed LNA Architecture

The proposed wideband LNA architecture is shown in Fig. 16. In this architecture, a wideband input matching network is designed using inductors L_e and L_b . The input matching network is similar to the one employed in narrowband approach at low-GHz range [29]; however as demonstrated later, the same components can be used for wideband matching at mm-wave frequencies using BiCMOS technology. The wideband gain is obtained using a proposed coupled-resonator as the load of each amplifier stage. Coupled-resonators can result in two peaks depending on their coupling coeffi-

cient. Cascading two of these coupled-resonators, with unequal peaking frequencies, results in a wideband response as discussed later. Two gain stages with two different coupled-resonator loads are implemented to provide the wideband response for the proposed LNA. In addition, these two stages increase the voltage gain across the desired wideband frequency range. Finally, the noise due to the cascode transistor is reduced by adding the inductor L_m to resonate with the parasitic capacitance at the emitter of Q_2 , c_{pm} [9, 39, 51]. Hence, the emitter of Q_2 is degenerated with a high impedance, and the noise current of Q_2 is not injected to the output of the first stage. Instead, the noise current circulates within Q_2 . All the above techniques enable the design of an LNA with a larger BW and higher gain, low wideband input referred noise and low power consumption.

a. Input Matching Network

The input matching network consists of the pad, inductors L_b and L_e , and the base-emitter capacitance, c_{be} , of Q_1 . The input matching network is similar to the narrow-band one at low-GHz frequencies. However, due to operation within K-band, it has a lower quality factor suitable for wideband matching at this frequency range. This effect is investigated using schematic-level simulations by only changing the inductance value of L_b using Spectre². The simulated return loss (S_{11}) is demonstrated in Fig. 17, where a sharper bandwidth is demonstrated for the low frequency range and a wider bandwidth is achievable at higher frequencies if the same capacitance (c_{be}) is assumed in both cases. The simple expression for the input impedance of this matching network at lower frequencies does not help to optimize its performance at mm-wave frequencies [29]. Therefore, the impact of parasitics on the input matching,

²Spectre 6.2, Cadence 2008

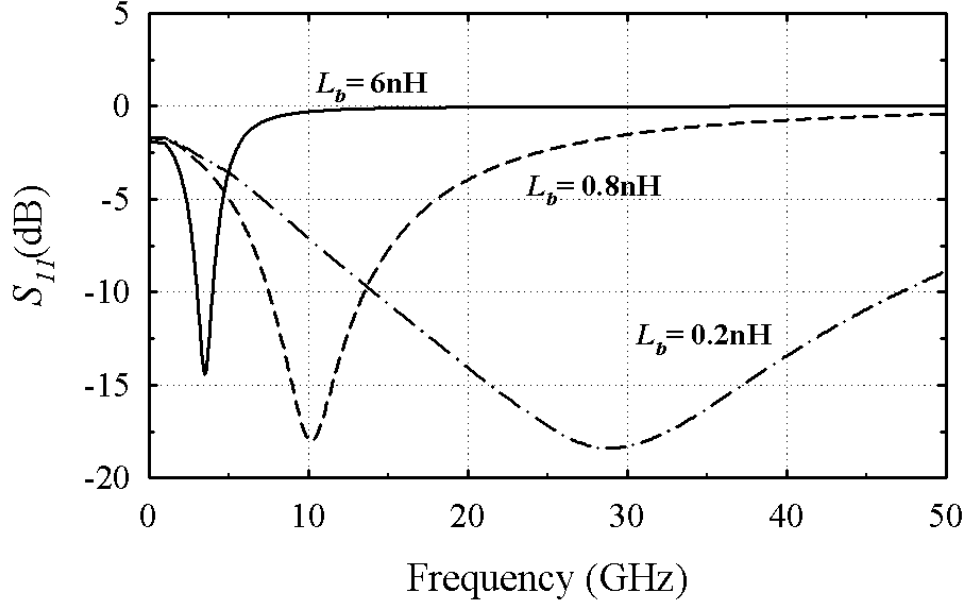


Fig. 17. Simulated input return loss of the matching network in Fig. 16 for different values of L_b .

are considered in details during the analysis as demonstrated below.

The equivalent circuit model of the wideband input matching network at the base of Q_1 is shown in Fig. 18, where the resistance R_q is equal to $\omega_T \cdot L_e$. The transistor Q_1 is sized such that c_{be} and L_e resonate at the mid-band of interest. C_{pad} and C_p are the capacitances due to the pad and miller reflected base-collector capacitance of Q_1 , respectively. The emulated resistance R_q provides the required $50\ \Omega$ input matching without increasing the overall NF . The wideband operation of the input matching network is explained by dividing it into two sections.

The first section, consisting of L_e , c_{be} , and R_q , forms a very low-Q ($Q < 1$) series RLC resonant circuit because of the large base-emitter capacitance of Q_1 and the operation at 23-32 GHz frequency range ($Q = \frac{1}{\omega c_{be} R_q}$). Inductors L_e and L_b should have high-Q to keep the overall NF low. Fig. 19 shows the simulated return loss of

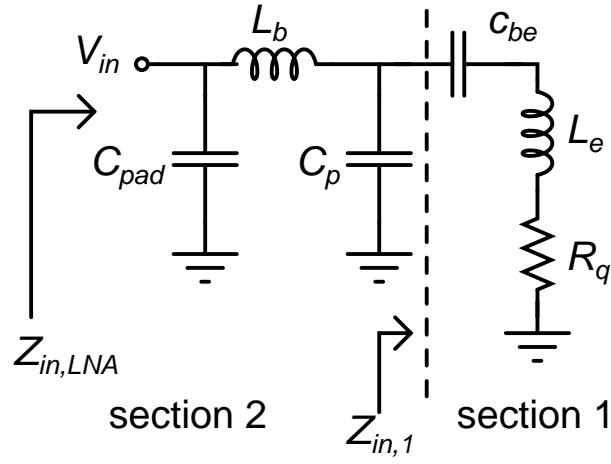


Fig. 18. Equivalent circuit model of the input matching network.

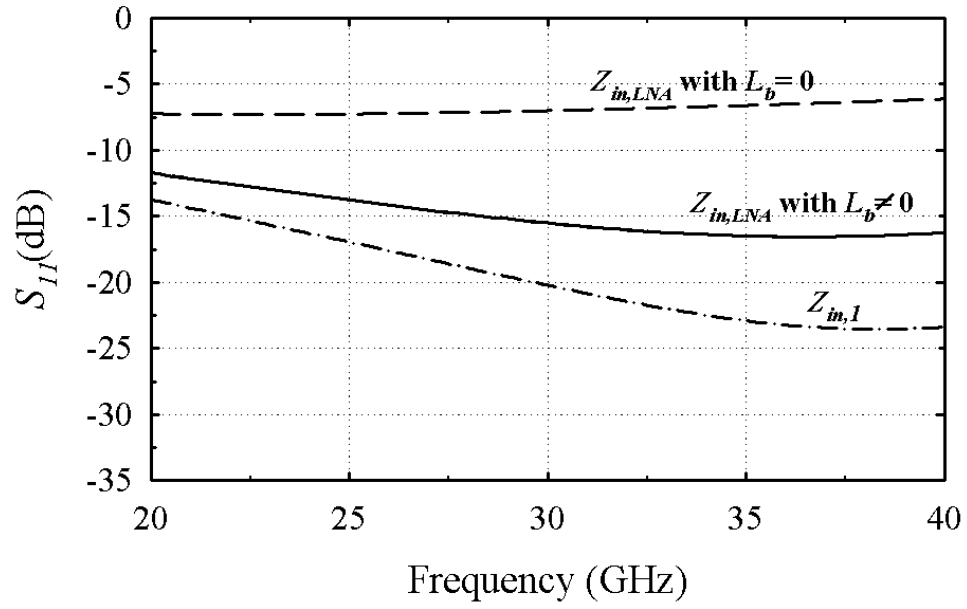


Fig. 19. Input return loss for $Z_{in,1}$ and $Z_{in,LNA}$ in Fig. 18 with and without L_b .

the first section. As depicted, matching better than -15 dB is achievable using L_e , c_{be} , and R_q across the band of interest. However without L_b , the parasitic capacitance, $C_p + C_{pad}$, changes the effective input impedance considerably, and poor matching is achieved as shown in Fig. 19. Finally, the inductor L_b recovers the matching by forming a low-Q pi-matching network with capacitors C_p and C_{pad} , as drawn in Fig. 18. The low quality factor of pi-matching network is because of the $50\ \Omega$ impedance seen at $Z_{in,1}$ and the operation within K-band.

The input impedance of the proposed LNA is then approximated by

$$\begin{aligned} Z_{in}(s) &\approx \frac{1 + sR_q c_{be} + s^2(L_e + L_b)c_{be} + s^3 R_q L_b c_{be} C_p}{sC_T(1 + s\frac{c_{be}}{C_T} R_q C_b + s^2 \frac{c_{be}}{C_T} (L_e C_p + L_b C_{pad}))}, \\ C_b &= C_p + C_{pad}, \\ C_T &= C_p + C_{pad} + c_{be}. \end{aligned} \tag{3.9}$$

For the low-GHz case, the coefficients of s^2 and higher are neglected. However at mm-wave frequencies, these coefficients are comparable to the first order term, and cannot be neglected. Eq. (3.9) also shows that L_b increases the magnitude of s^2 and s^3 coefficients in the numerator, therefore, zeros are moved to a lower frequency to cancel the effect of poles allowing wider input matching bandwidth. This effect and the lower quality factor enables the design of a wideband input matching network.

b. Wideband Load

The wideband load is achieved using coupled-resonator structure, shown in Fig. 20(a). The input impedance of the coupled-resonator, Z_{load} , is found by considering the equivalent circuit model shown in Fig. 20(b). Assuming a tank circuit with high quality factor and resonators with similar component values, the input impedance,

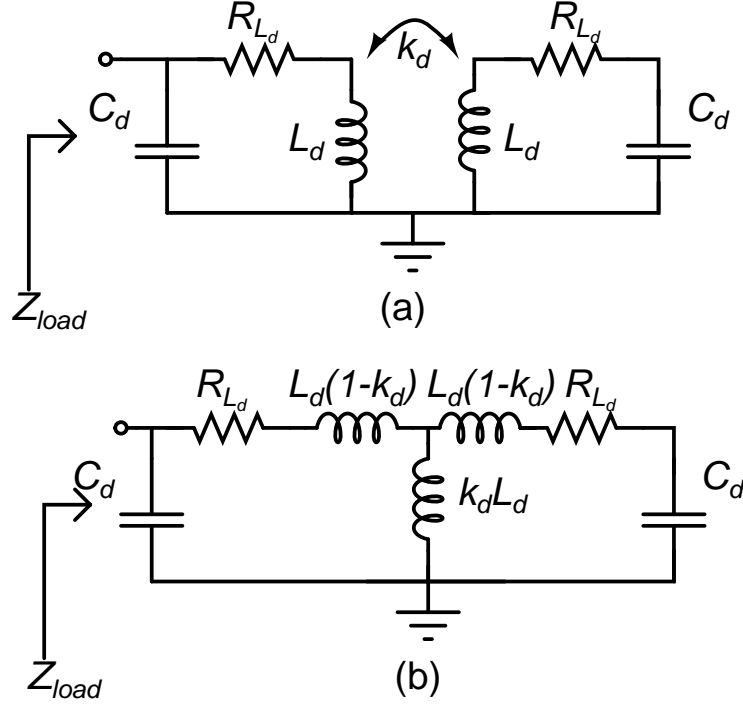


Fig. 20. (a) Coupled-resonator structure as the load of each stage (b) equivalent circuit model of each coupled-resonator.

Z_{load} , is approximated as follows [52]

$$\begin{aligned}
 Z_{load}(\omega) &\approx R_{L_d} \frac{N(\omega)}{D(\omega)}, \\
 N(\omega) &= \left\{1 - 2\left(\frac{\omega}{\omega_o}\right)^2\right\} + j\left\{Q_{L_d}\left(\frac{\omega}{\omega_o}\right)\left(1 - (1 - k_d^2)\left(\frac{\omega}{\omega_o}\right)^2\right)\right\}, \\
 D(\omega) &= \left\{\left(1 - \left(\frac{\omega}{\omega_o}\right)^2\right)^2 - \frac{\left(\frac{\omega}{\omega_o}\right)^2}{Q_{L_d}^2} - k_d^2\left(\frac{\omega}{\omega_o}\right)^4\right\} + j\left\{\frac{2\left(\frac{\omega}{\omega_o}\right)}{Q_{L_d}}\left(1 - \left(\frac{\omega}{\omega_o}\right)^2\right)\right\}.
 \end{aligned} \tag{3.10}$$

where k_d is the coupling coefficient between two resonators, ω_o is the resonant frequency of a single resonator defined as $\omega_o = 1/\sqrt{L_d C_d}$, and Q_{L_d} is the quality factor of a single tank circuit defined as $Q_{L_d} = \frac{\omega_o L_d}{R_{L_d}}$. Eq. (3.10) shows that the load impedance has two peaks as demonstrated by Fig. 21(a). These two peaks are found by solving

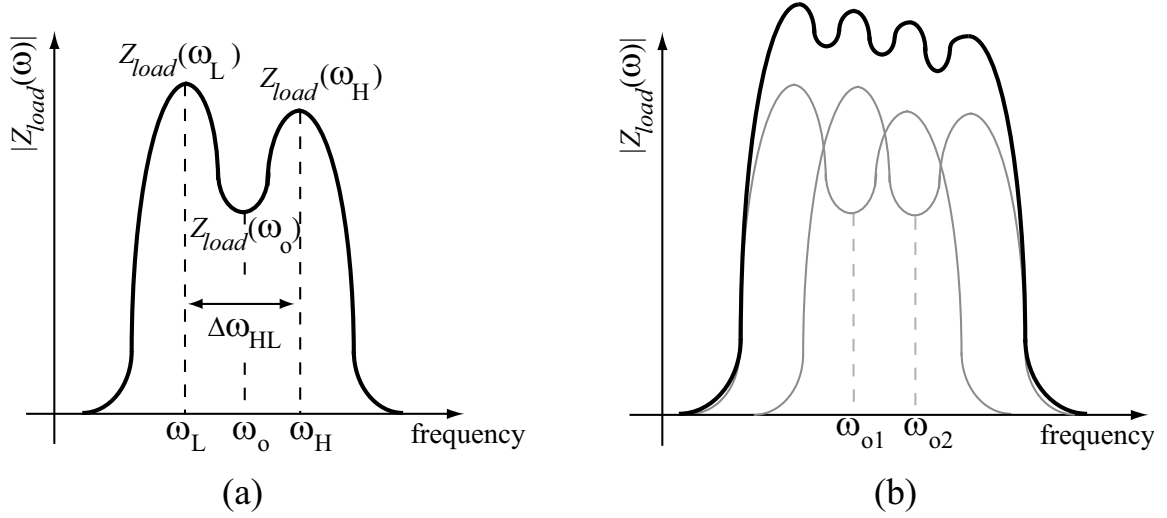


Fig. 21. (a) Magnitude response of the input impedance of coupled-resonator in Fig. 20, (b) Magnitude response of the input impedance of two cascaded coupled-resonator.

$Im\{\frac{1}{Z_{load}}\} = 0$ for the parallel resonant circuit, and are located at

$$\frac{\omega_{H,L}}{\omega_o} = \sqrt{1 \pm k_d}. \quad (3.11)$$

Hence, the two peak frequencies are separated by

$$\Delta\omega_{HL} = (\sqrt{1 + k_d} - \sqrt{1 - k_d})\omega_o \approx k_d\omega_o. \quad (3.12)$$

The approximation in (3.12) is valid for a wide range of k_d (for $k_d \leq 0.7$ the error in $\Delta\omega_{HL}$ calculation is less than 5%). The resonator impedance values at peak frequencies, ω_L and ω_H , are given by

$$Z_{load}(\omega_{H,L}) = R_{Ld}Q_{Ld}^2 \frac{(k_d^2 \pm k_d - 1)^2(1 \pm k_d)}{k_d^2 \pm 2k_d + 2}. \quad (3.13)$$

Eq. (3.13) shows that the impedance at the high peak frequency, ω_H , is lower

than the one at ω_L as demonstrated in Fig. 21(a). Dual-band and wideband loads can be obtained using the coupled-resonator circuit architecture as shown in Fig. 21. Using a single coupled-resonator, the two peak frequencies could be adjusted to resonate at the targeted frequencies leading to dual-band response. On the other hand, wideband operation is achieved by cascading two coupled-resonators as demonstrated in Fig. 21(b). The two coupled-resonators are tuned at two different center frequencies (ω_{o1} and ω_{o2}) to provide the required wideband operation.

To minimize the in-band ripples, the maximum to minimum in-band load variations should be reduced. The minimum in-band load of a single coupled-resonator is found by evaluating (3.10) at $\omega = \omega_o$ yielding

$$|Z_{load}(\omega_o)| = \frac{R_{Ld}Q_{Ld}^2}{1 + k_d^2Q_{Ld}^2}. \quad (3.14)$$

Therefore, the maximum to minimum overall gain variations across the band is found from (3.13) and (3.14) as follows

$$\frac{|Z_{load}(\omega_L)|}{|Z_{load}(\omega_o)|} \approx \frac{(k_d^2 - k_d - 1)^2(1 - k_d)}{k_d^2 - 2k_d + 2}(1 + k_d^2Q_{Ld}^2). \quad (3.15)$$

Typically, $\frac{|Z_{load}(\omega_L)|}{|Z_{load}(\omega_o)|}$ should be limited to a value lower than 6 dB to reduce the ripples. For a specific value of the coupling coefficient, the maximum variation imposes an upper value for the quality factor as depicted by (3.15). Increasing Q_{Ld} increases the maximum to minimum load variations as demonstrated in Fig. 22 using circuit-level simulations. For $k_d = 0.19$, Q_{Ld} should be lower than 8 to reduce the variations. It is important to note that increasing k_d places the two resonant frequencies further apart, however lower value of Q_{Ld} (lower gain) is necessary to reduce the in-band variations. Therefore, there is a trade-off between flat bandwidth extension and overall gain of the amplifier. As an example, increasing k_d by 50% increases the bandwidth by the same amount (according to (3.12)), however this

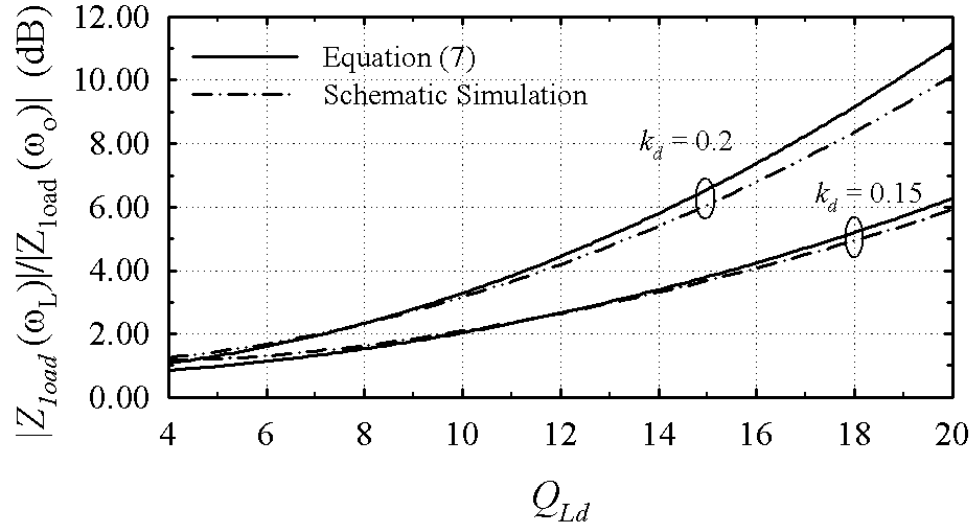


Fig. 22. Circuit-level simulations of $\frac{|Z_{load}(\omega_L)|}{|Z_{load}(\omega_o)|}$ versus Q_{Ld} for different values of k_d .

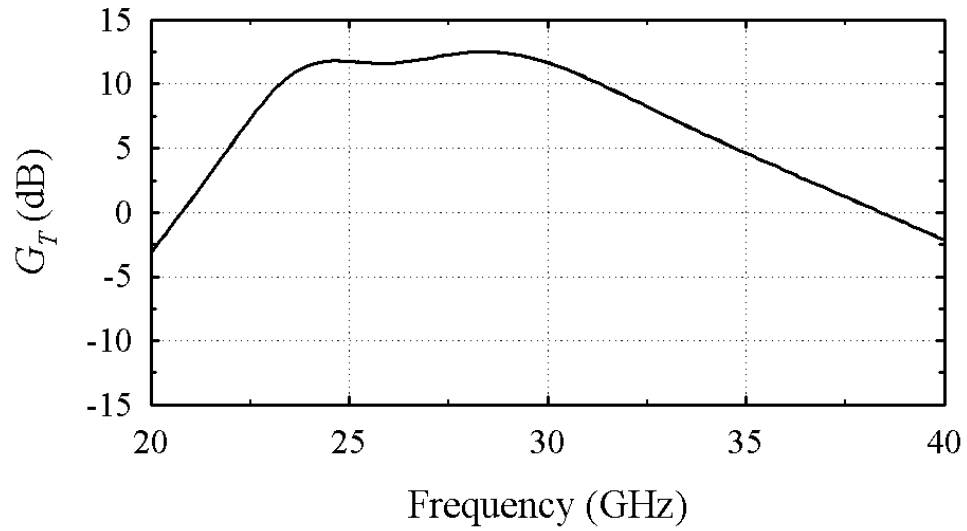


Fig. 23. The simulated total gain of the LNA demonstrating the effect of cascading two coupled-resonators as loads of stages 1 and 2 in Fig. 16.

increase requires reducing Q_{Ld} to 5, hence reducing the gain by almost 50%.

Fig. 23 demonstrates the simulated gain of two cascaded amplifiers with coupled-resonator loads shown in Fig. 16. The total gain, G_T , of the cascaded amplifier is given by

$$G_T = (G_{meff,1}Z_{load,1}) \cdot (G_{meff,2}Z_{load,2}), \quad (3.16)$$

where $G_{meff,1}$ and $G_{meff,2}$ are the effective transconductance of each gain stage. In this simulation, a coupling coefficient of 0.19 is assumed to cover the required band. The first and second coupled-resonators are designed with ω_{o1} , ω_{o2} of 26 and 28 GHz, respectively. The two center frequencies are selected such that the overall response leads to the desired wideband response to cover the 23-32 GHz frequency band. As discussed earlier, the in-band ripples are reduced by selecting Q_{Ld} to be lower than 8. In addition, $G_{meff,1}$ smoothens the gain through the inductor L_m in Fig. 16. Inductor L_m forms a wideband parallel RLC resonant circuit with its peak frequency adjusted at the highest operating frequency. This resonant circuit boosts the gain at higher frequencies, leading to flatter-wideband gain.

c. Noise Analysis

The total input referred noise of the proposed LNA is mainly dominated by the first stage according to Friis equation [34]. As a result, it is assumed that the overall noise figure is mainly due to the first stage in the following analysis. Fig. 24 shows the equivalent noise circuit of the first amplifier stage. The base and collector noise currents of Q_1 , noise due to parasitic base resistances of Q_1 , R_b , and noise due to losses of L_b , R_{Lb} , and L_e , R_{Le} , are considered in this equivalent model. The noise due to the cascode transistor, Q_2 , is considerably reduced by adding the inductor L_m , and as a result, it can be neglected in the following analysis.

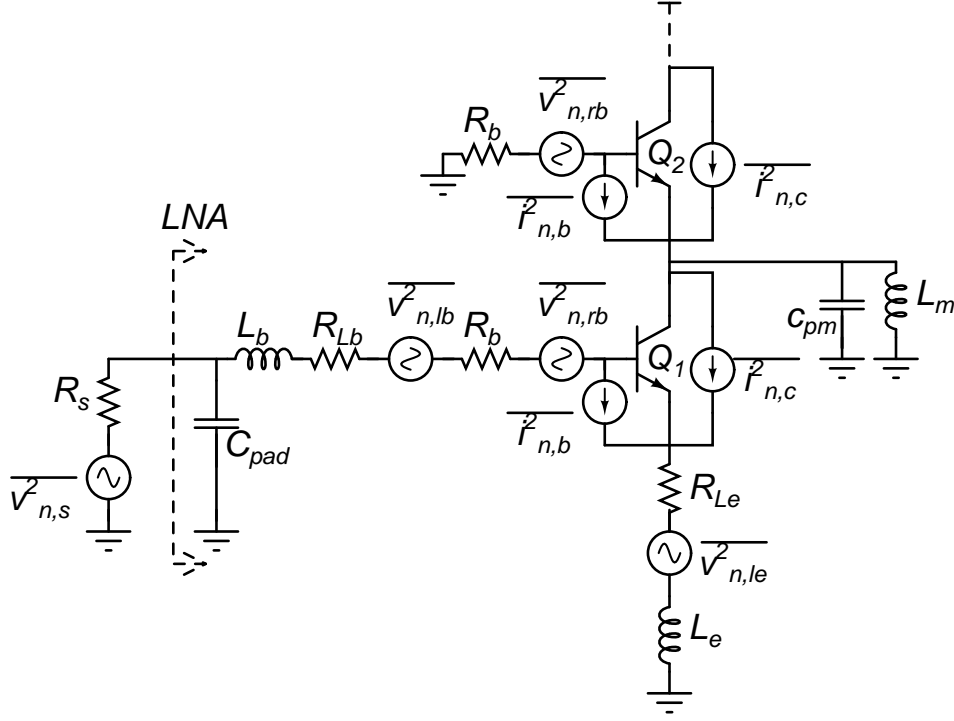


Fig. 24. Main noise sources of the proposed wideband LNA.

Noise of Q_1 : The equivalent input referred noise due to the base and collector noise currents of Q_1 are given by

$$\frac{\overline{v_{ni,Q1ib}^2}}{\overline{i_{n,b}^2}} \approx \quad (3.17)$$

$$\left| \frac{g_{m1}(R_s + R_b + R_{Le}) + s g_{m1}(L_e + L_b + R_s(R_{Le} + R_b)C_{pad}) + s^2 g_{m1} R_s C_{pad}(L_b + L_e)}{g_{m1} - s c_{bc} + s^2 c_{bc} g_{m1} L_e} \right|^2,$$

$$\frac{\overline{v_{ni,Q1ic}^2}}{\overline{i_{n,c}^2}} \approx \quad (3.18)$$

$$\left| \frac{1 + s(R_s + R_b)(c_{bb} + C_{pad}) + s^2 c_{bb}(L_e + L_b + R_s R_b C_{pad}) + s^3 C_{pad} R_s L_b c_{bb}}{g_{m1} - s c_{bc} + s^2 c_{bc} g_{m1} L_e} \right|^2,$$

$$c_{bb} = c_{be} + c_{bc}.$$

where $s = j\omega$, R_s is the source resistance, and g_{m1} is the transconductance of Q_1 .

$\overline{i_{n,b}^2}$ and $\overline{i_{n,c}^2}$ are the base and collector noise currents of Q_1 , and are given by

$$\overline{i_{n,b}^2} = 2qI_{B1}, \quad (3.19)$$

$$\overline{i_{n,c}^2} = 2qI_{C1} \quad (3.20)$$

where q is the electron charge constant, I_{B1} is the base current, and I_{C1} is the collector current of Q_1 .

Higher order coefficients of s are not neglected in (3.17) and (3.18) because these terms are effective across the band of interest. Eqs. (3.17) and (3.18) show that the input referred noise of Q_1 increases proportionally with the value of L_b at higher frequencies. This is because the voltage gain between the input and the base-emitter junction of Q_1 is inversely proportional to L_b . Due to the matching requirements, shown in (3.9), L_b cannot be set to zero to lower the noise. Therefore, there is a tradeoff between the input matching and noise figure for this amplifier. In this design, L_b is selected such that the input return loss is better than -12 dB across the band of interest.

The total input referred noise voltage due to Q_1 , $\overline{v_{ni,Q_1}^2}$, is given by adding the two expressions in (3.17) and (3.18). The resultant total input referred noise

normalized to the noise voltage of the source resistance can be approximated by

$$\begin{aligned}
\frac{\overline{v_{ni,Q1}^2}}{4kTR_s\Delta f} &\approx \frac{\eta_1(\omega)}{g_{m1}} + \eta_2(\omega)g_{m1}, \\
\eta_1(\omega) &= \frac{|1 - (\frac{\omega}{\omega_1})^2 + j\frac{\omega}{\omega_2}(1 - (\frac{\omega}{\omega_3})^2)|^2}{2R_s}, \\
\eta_2(\omega) &= \frac{|1 - (\frac{\omega}{\omega_2})^2 + j\frac{\omega}{\omega_4}|^2(R_s + R_b)^2}{2\beta R_s}, \\
\omega_1 &= \sqrt{\frac{1}{(c_{be} + c_{bc})(L_b + L_e + R_s R_b C_{pad})}}, \\
\omega_2 &= \sqrt{\frac{R_s + R_b}{C_{pad}(L_b + L_e)R_s}}, \\
\omega_3 &= \frac{1}{(c_{be} + c_{bc} + C_{pad})(R_s + R_b)}, \\
\omega_4 &= \frac{R_s + R_b}{L_e + L_b + R_s R_b C_{pad}}.
\end{aligned} \tag{3.21}$$

where k is Boltzmann constant, T is the temperature in kelvin, ω is the operating frequency in radian/s, and β is the current gain of BJT. Eq. (3.21) shows that the total input referred noise voltage due to the collector noise current can be decreased by increasing the value of g_{m1} . However, increasing g_{m1} increases the contribution of the base noise current. Hence, there is an optimum value for g_{m1} to minimize the total input referred noise due to Q_1 . By differentiating (3.21) with respect to g_{m1} and equating the resultant expression to zero, $g_{m1,opt}$ is given by

$$g_{m1,opt} = \sqrt{\frac{\eta_1(\omega)}{\eta_2(\omega)}}. \tag{3.22}$$

The minimum input referred noise due to Q_1 is then as follows

$$\frac{\overline{v_{ni,Q1}^2}}{4kTR_s\Delta f}|_{min} = 2\sqrt{\eta_1(\omega)\eta_2(\omega)}. \tag{3.23}$$

Eq. (3.22) shows that $g_{m1,opt}$ depends on the operating frequency because η_1 and η_2 are both frequency dependent. Fig. 25 shows the value of $g_{m1,opt}$ versus the oper-

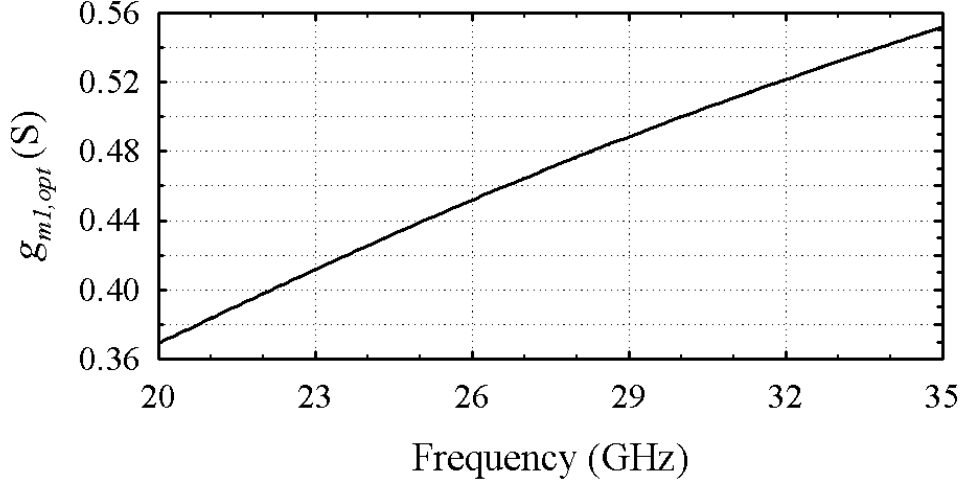


Fig. 25. Optimum transconductance due to Q_1 ($g_{m1,opt}$) versus the operating frequency.

ating frequency. As depicted, $g_{m1,opt}$ varies from 0.4-0.5 S for 23-32 GHz frequency range, which means that $g_{m1,opt}$ does not vary significantly across the band of interest.

The input referred noise voltage due to Q_1 , defined in (3.21), is drawn versus g_{m1} in Fig. 26. At $g_{m1,opt} = 0.45 S$ the noise voltage is minimum, as given by (3.23). In addition, the noise voltage slightly changes from a transconductance value of 0.15 S when compared to the optimum value at 0.45 S . Choosing a value for g_{m1} lower than optimum reduces the power consumption with a slight increase in the input referred noise voltage due to Q_1 . In this design, g_{m1} is selected to be 0.18 S to reduce the power consumption of the LNA.

Noise of Cascode Transistor: At low-GHz frequencies the noise contribution of the cascode transistor, Q_2 , is neglected because of the high degeneration resistance at the emitter of Q_2 . However at mm-wave frequencies, the parasitic capacitance at the emitter of Q_2 reduces the degeneration impedance. As a result, most of the noise due to Q_2 appears at the output of the first stage and increases the overall noise figure

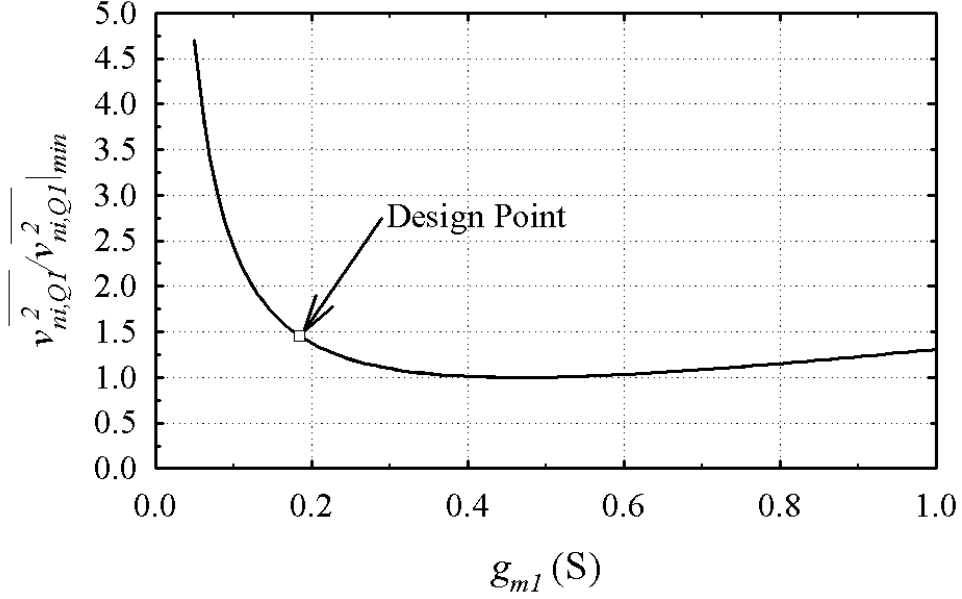


Fig. 26. Normalized input referred noise voltage of Q_1 versus g_{m1} .

(NF). To overcome this problem, the inductor, L_m , is added to resonate with the parasitic capacitance to increase the degeneration impedance of Q_2 [9, 39, 51]. As a result, the noise of Q_2 does not appear at the output of the first stage.

Also, the current source, consisting of M_{p1} in Fig. 16, is added to control the quality factor of the tank circuit (L_m and parasitic capacitance) to provide a wideband noise reduction of Q_2 at mm-wave frequencies. The quality factor is adjusted by changing the current passing through Q_2 , and hence its transconductance, g_{m2} . The resonant frequency and quality factor of this tank circuit are adjusted to be 29 GHz and 3, respectively, to cover the entire bandwidth.

Overall Noise Figure: The total noise figure, NF_{tot} , of the proposed LNA is mainly due to the noise of the first stage as discussed earlier in this section, and

is given by

$$NF_{tot}(\omega) = 1 + \frac{R_{Lb} + R_b}{R_s}(1 + \omega^2 C_{pad} R_s) + \frac{\eta_1(\omega)}{g_{m1}} + \eta_2(\omega) g_{m1}, \quad (3.24)$$

Eq. (3.24) shows that the input referred noise of the base resistance of Q_1 , R_b , and loss resistance of L_b , R_{Lb} , increase as the frequency increases due to the presence of the pad capacitance, C_{pad} . This capacitance produces a pole at the input of the LNA and increases the noise contributed by R_b and R_{Lb} at higher frequencies, as shown in (3.24). In this design, the pole ($1/C_{pad}R_s$) exists around 31 GHz, which increases the input referred noise due to R_b and R_{Lb} by 3 dB at 31 GHz. It is difficult to increase this pole because the source resistance is fixed and pad size is limited by the minimum size provided by the technology. Eq. (3.24) also demonstrates that NF_{tot} increases with increasing the value of L_b as well as R_{Lb} , therefore L_b cannot be increased freely to provide better matching.

d. Linearity Analysis

According to Friis equation [34], the input referred third order intercept point (IIP_3) of the wideband LNA is defined as follows

$$\frac{1}{IIP_{3,tot}} = \frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}}. \quad (3.25)$$

where G_1 is the gain of the first stage, and $IIP_{3,tot}$, $IIP_{3,1}$, and $IIP_{3,2}$ are the total, first, and second stage input referred third order intercept point, respectively. For cascaded amplifiers, $IIP_{3,tot}$ is mainly determined by the last stage. However in the proposed LNA, the first stage is implemented using a bipolar transistor (BJT), while the second stage is implemented using MOS transistor. The linearity of the MOS

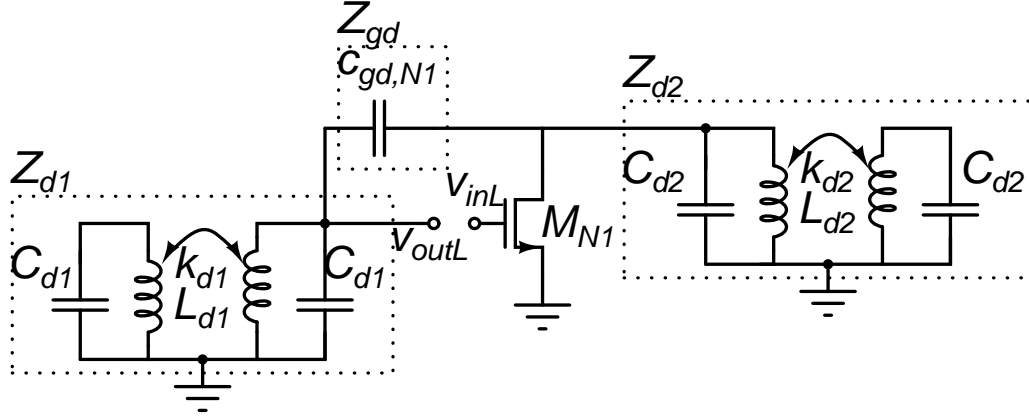


Fig. 27. Equivalent model of the second stage demonstrating the input/output tuned loads.

transistor is higher than the BJT, and therefore, the linearity is determined by both stages. This is demonstrated by noting that the linearity of the first stage is around -2 dBm, and it provides a maximum gain of ($G_1 = 9$ dB). The linearity of the second stage is higher than 7 dBm. Hence, the second term in (3.25) is comparable to the first term, and therefore the linearity of both stages is considered. In case of replacing the MOS transistor with a BJT one, $IIP_{3,tot}$ will be reduced.

e. Design for Stability

Stability is one of the important design targets at mm-wave frequencies. For a single transistor the feedback gate-drain capacitance may lead to instability for the case of having a tank circuit at the input and output of the amplifier. The first stage of the LNA is implemented using a cascode architecture to solve this problem [53]. However, a common source configuration is used for the second stage, which may lead to instability if not carefully designed. Stability puts an upper limit for the gain to avoid the unnecessary oscillations. Fig. 27 shows the equivalent circuit used

for studying the stability, where v_{inL} and v_{outL} are the input and output voltages of the loop, and Z_{d1} and Z_{d2} are the coupled resonators of the first and second stage, respectively. The loop gain, G_L , for this architecture is given by

$$G_L = \frac{v_{outL}}{v_{inL}} = -\frac{g_{m,N1}}{\frac{1}{Z_{d1}} + \frac{1}{Z_{d2}} + \frac{Z_{gd}}{Z_{d1}Z_{d2}}}, \quad (3.26)$$

where $g_{m,N1}$ is the transconductance of MOS transistor, and Z_{gd} is the impedance of gate-drain capacitance, $c_{gd,N1}$ of MOS transistor. The condition at which oscillation may occur is obtained by placing the imaginary part in (3.26) to zero, i.e.

$$\text{Im}\left\{\frac{1}{Z_{d1}} + \frac{1}{Z_{d2}} + \frac{Z_{gd}}{Z_{d1}Z_{d2}}\right\} = 0. \quad (3.27)$$

Eq. (3.27) gives the frequency at which the oscillation may happen. Based on circuit-level simulations, the oscillation may occur at a frequency around 18 GHz in this design. To guarantee that the oscillation will not start, the loop gain has to be lower than one at this frequency, hence placing an upper limit for the value of $g_{m,N1}$ in (3.26). Fig. 28 shows the loop gain versus $g_{m,N1}$ at the unstable frequency. In this simulation, it is assumed that $c_{gd,N1}$ scales proportionally with $g_{m,N1}$. For values of $g_{m,N1}$ lower than 50 mS the second stage is stable. In this design, $g_{m,N1}$ is selected to be 20 mS to reduce the input capacitance of M_{N1} , and therefore the second stage provides a peak gain of 5 dB at the lower peak frequency of the coupled resonator.

2. Inductor Layout

The performance of the mm-wave integrated circuits mainly depends on the parasitics of routing paths and the quality factor of the passive components. Poor quality factor and the parasitic inductance introduced by routing paths can greatly limit the

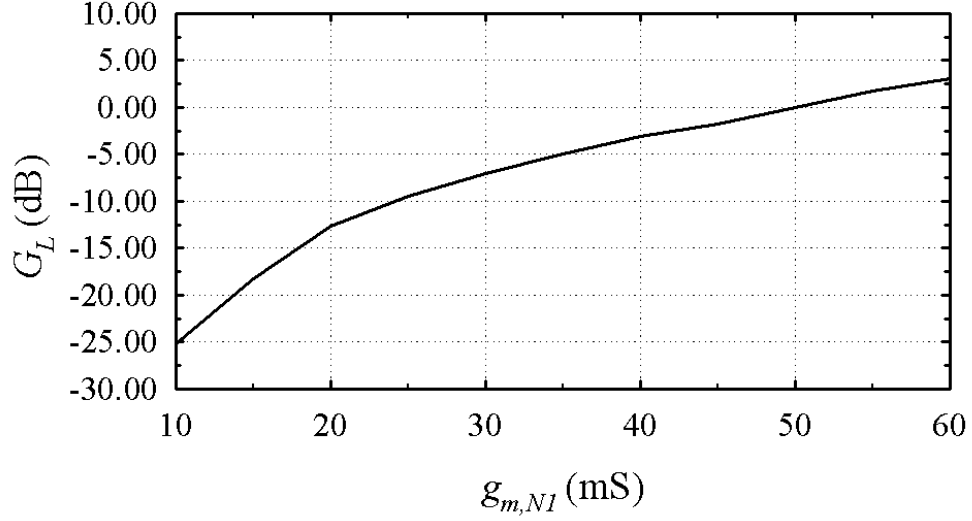


Fig. 28. Loop gain, G_L , versus $g_{m,N1}$ at the resonance frequency of tuned input/output second stage in Fig. 27.

performance. An electromagnetic simulator, SONNET³, is used to model the various non-ideal passive effects. Inductors L_b and L_e are implemented using microstrip transmission line (MTL) structures, while the coupled inductor L_d is implemented using a center-tapped differential inductor. The inductor L_m is implemented using the conventional spiral inductor structures. All the inductors are realized with the thickest top metal layer which is farthest from the substrate to reduce losses.

Microstrip structures are used for L_b (and L_e) implementation, as shown in Fig.29(a), because they are characterized by their high quality factor compared to the normal spiral inductors. Higher quality factor reduces the noise introduced by the input matching network. The width of the transmission line is increased to reduce the losses. The self resonant frequency of the inductor limits the width of the MTL structure.

³Sonnet Inc. www.sonnet.com

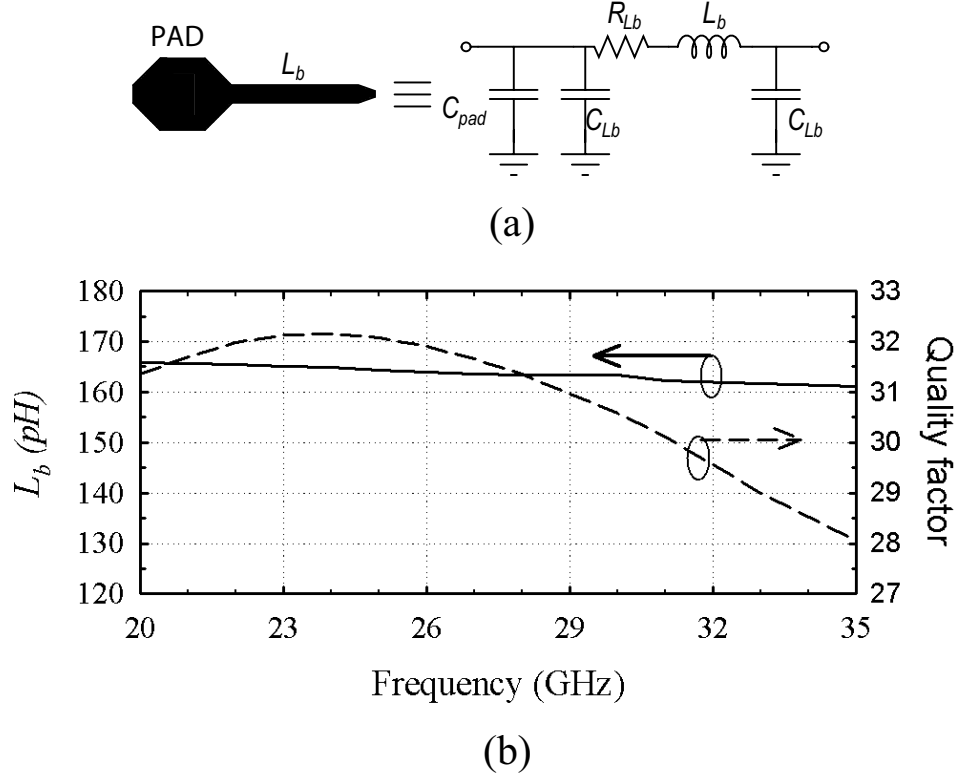


Fig. 29. (a) Layout of L_b (and L_e) using MTL, (b) Inductance value and quality factor of L_b versus frequency using SONNET.

Electromagnetic simulations using SONNET show a line width of $20 \mu\text{m}$ increases the NF only by 0.2-0.3 dB compared to a lossless line while providing maximum quality factor in the band of interest. Fig.29(b) shows the simulated inductance and quality factor of the designed MTL inductor L_b . An inductance of 160 pH with a quality factor higher than 28 is obtained within the desired frequency band.

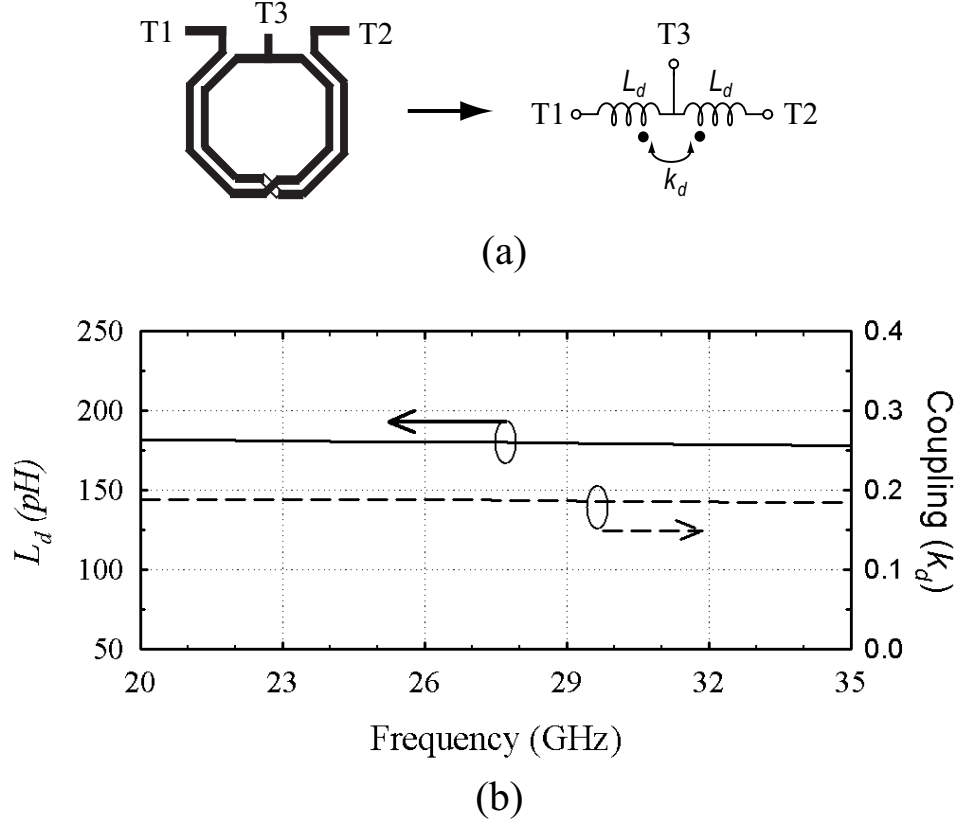


Fig. 30. (a) Layout of L_d using a center-tapped differential inductor , (b) Inductance value and coupling coefficient, k_d , for coupled-inductor, L_d , versus frequency using SONNET.

The coupled inductors, L_d , is implemented using a center-tapped differential inductor as shown in Fig. 30(a). The line width and spacing between the two inductors are optimized to achieve a coupling coefficient of 0.19. According to (3.12) this coupling coefficient separates the two peak frequencies of each load by 4.9 and 5.3 GHz for a center frequency of 26 and 28 GHz, respectively. Hence, the resultant 3-dB bandwidth is around 9 GHz. The simulated inductance value and coupling coefficient for the coupled inductor are shown in Fig. 30(b). Both values are almost constant along the frequency band of interest. This is because the self resonant frequency of

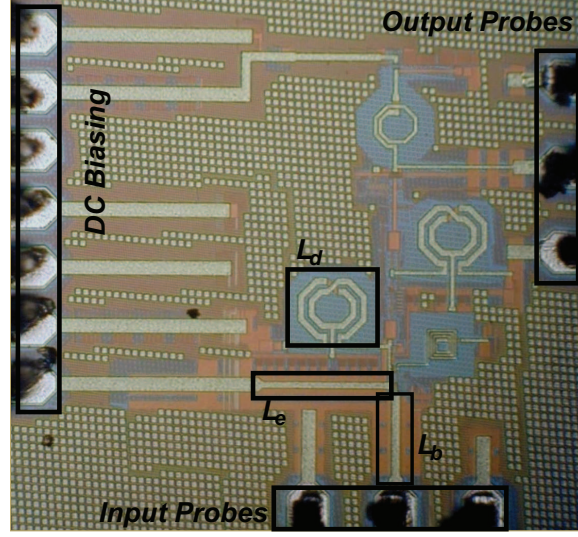


Fig. 31. Die-photo of the wideband LNA with an area of 0.25 mm^2 (pads and buffer are not included).

the differential inductor is placed at a higher frequency.

3. Simulation and Experimental Results

The wideband LNA is fabricated using $0.18 \text{ }\mu\text{m}$ BiCMOS technology provided by Jazz Semiconductor. The die micrograph is shown in Fig. 31, where the total area is 0.25 mm^2 , excluding pads and output buffer. The mm-wave input, output and DC biasing signals are applied and monitored using on-wafer probing to reduce the losses and mismatches introduced by the measurement setup. Ground-Signal-Ground (GSG) probes are used to apply and measure the mm-wave signals, and an 8 pin DC probe is used to apply the required DC biasings. The effect of the output buffer is de-embedded from the LNA+Buffer measurements. The buffer is added at the output of the LNA to drive the $50 \text{ }\Omega$ input impedance of the network analyzer.

The circuit S-parameters are measured using Agilent N5230A network analyzer.

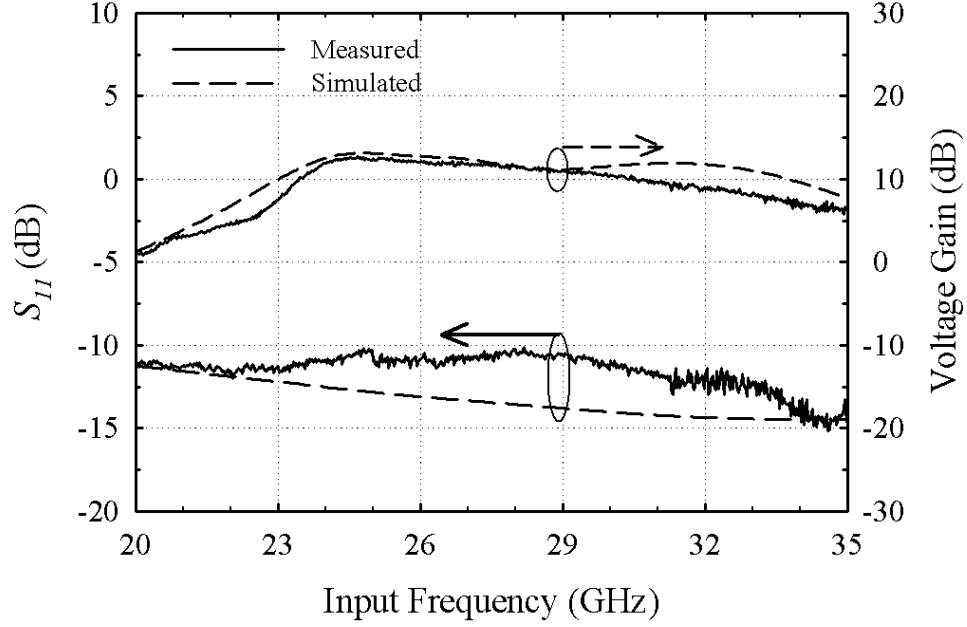


Fig. 32. Measured and simulated S_{11} and voltage gain of the proposed wideband LNA.

Fig. 32 shows the simulated and measured S_{11} of the amplifier. Measured S_{11} is lower than -12 dB for the entire 23-32 GHz frequency range. The simulated and measured voltage gain after de-embedding the buffer effect are also shown in Fig. 32. The buffer was designed to drive the 50 Ω impedance of network analyzer and a measured S_{22} better than -14 dB across the band of interest is obtained as shown in Fig. 33. The effect of buffer is de-embedded from measurements by simulating its introduced loss and subtracting results from measured S_{21} . The measured voltage gain is 12 dB with a 3-dB bandwidth of 9 GHz (Fig. 32). The simulated bandwidth is 11.5 GHz. The difference between the simulated bandwidth and measured one could be due to the non-accurate models of the transistors that may lead to extra capacitance, and/or the effect of process variation. The measured reverse isolation, S_{12} , is less than -35 dB over the entire band (Fig. 33). The measured phase and group delay are shown

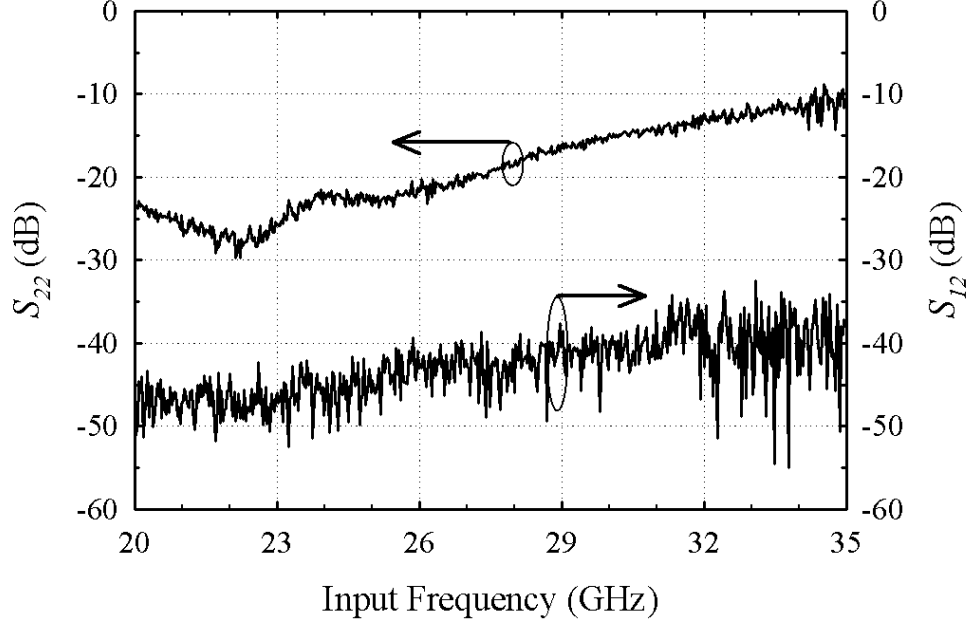


Fig. 33. Measured S_{22} of the buffer and reverse isolation S_{21} of the wideband LNA.

in Fig. 34. The measured noise figure versus the frequency is shown in Fig. 35, where the noise figure varies from 4.5 to 6.3 dB.

A two-tone IIP_3 measurement is performed for the LNA and the results are shown in Fig. 36 for the 23-32 GHz frequency range. The two tones are applied with the same amplitude and a frequency offset of 10 MHz. The measured IIP_3 changes from -4.5 to -6.3 dBm across the entire frequency range. The measured IIP_3 has two minima at 25 and 29 GHz. These two minima appear at the peak frequencies of the first stage coupled-resonator load.

The LNA consumes 13 mW from a 1.5 V supply, and each gain stage consumes the same amount of power. The performance of the proposed wideband LNA and comparison with other existing wideband LNAs around the same frequency range are summarized in Table VII. The proposed LNA achieves the highest bandwidth, com-

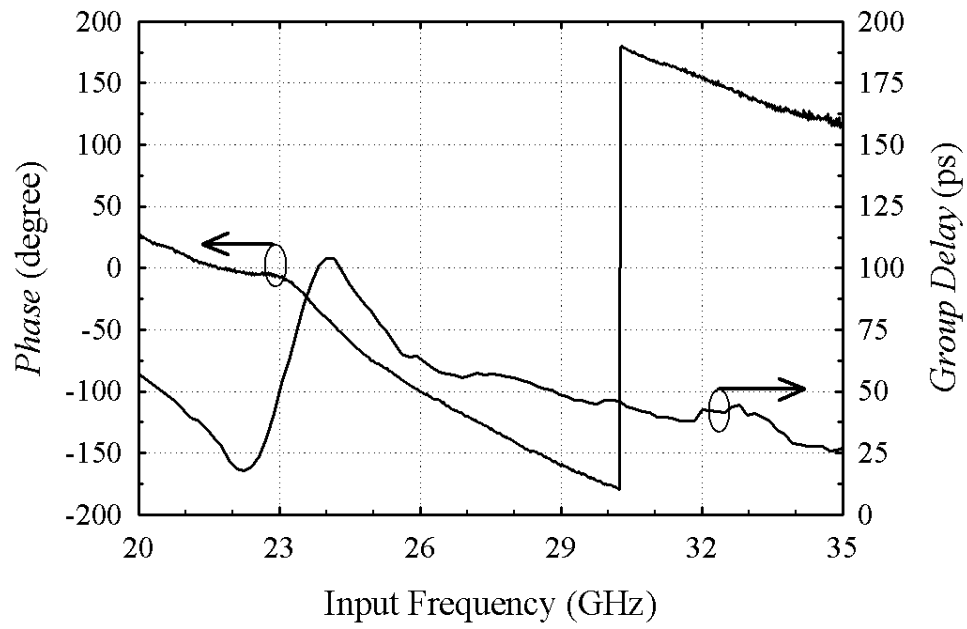


Fig. 34. Measured phase and group delay of the proposed wideband LNA.

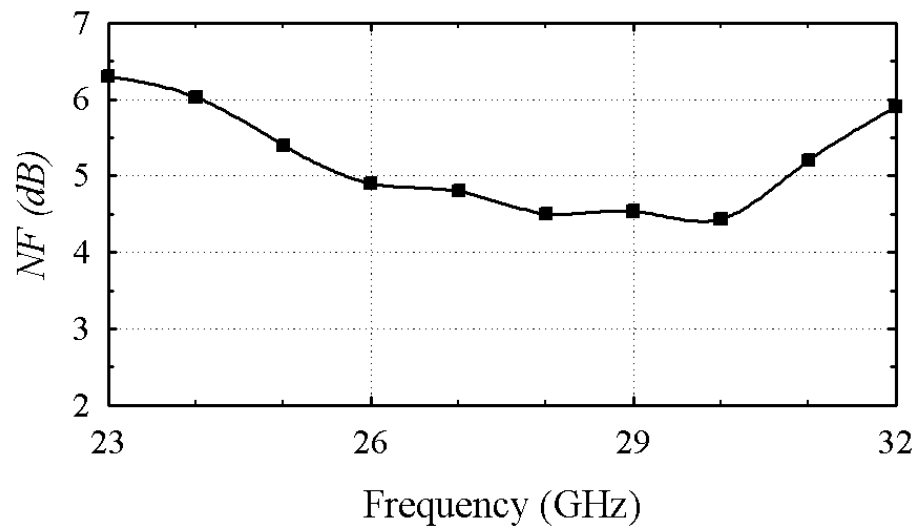


Fig. 35. Measured noise figure versus operating frequency.

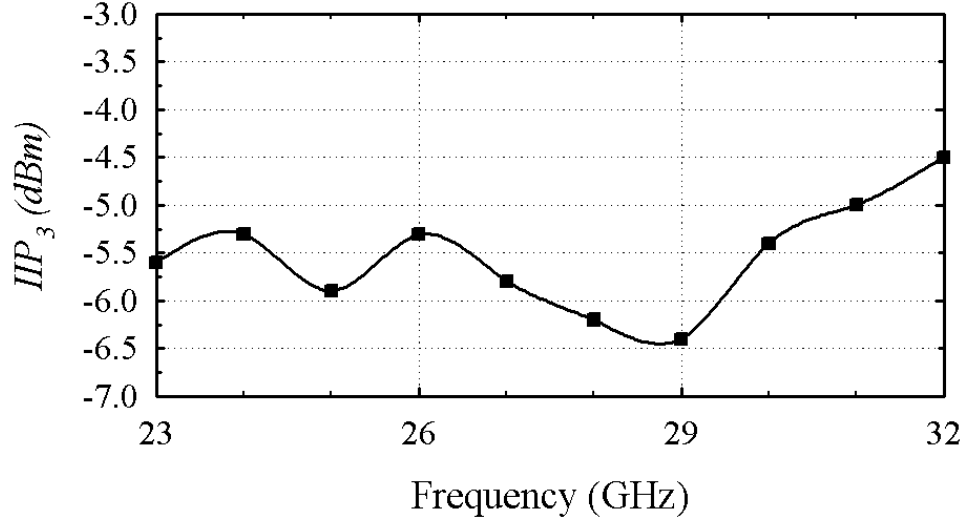


Fig. 36. Measured IIP_3 versus the operating frequency.

parable NF , IIP_3 and gain, while consuming less amount of power and operating at a higher frequency range. To compare different topologies and remove the technology dependency, the figure of merit, FOM , in [54] is modified and is given by

$$FOM = \frac{IIP_{3,av}[mW] \cdot Gain[abs] \cdot BW[GHz] \cdot f_{center}[GHz]}{(NF_{av} - 1)[abs] \cdot P_{DC}[mW] \cdot f_T^2[GHz]^2}, \quad (3.28)$$

where $IIP_{3,av}$ is the average input referred third order intercept point, NF_{av} is the average noise figure, P_{DC} is the DC power, BW is the bandwidth, and f_{center} is the center frequency. The proposed FOM exhibit a factor of 2.4 better than the best previously reported results in [49] for low-cost CMOS/BiCMOS technologies.

Table VII. Performance summary of the proposed mm-wave wideband LNA and comparison with the existing work.

Ref.	RF Freq. (GHz)	BW (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)	S11 (dB)	P_{DC} (mW)	f_T (GHz)	A. Area (mm ²)	Technology	FOM
[47]	18.6-26.3	7.7	4.4-5.4	12.9	NA	(-20)-(-5)	16.8	85	0.30	0.13 μm CMOS	NA
[48]	26-33.5 ^b	7.5 ^b	5-8.6 ^b	30 ^b	NA ^c	<-8	20	205	0.28	0.13 μm SiGe:C HBT BiCMOS	NA
[49]	21-27	6	4.9-6.1	9	-4 (@ 24GHz)	<-13	27	55 ^a	0.39	0.18 μm CMOS	$7.7 \cdot 10^{-4}$
[50]	22-29	7	4.5-6	18	NA	<-15	15	55	NA	0.18 μm CMOS	NA
This work	23-32	9	4.5-6.3	12	(-4.5)-(-6.3)	<-12	13	70	0.25	0.18 μm BiCMOS	$18.8 \cdot 10^{-4}$

^a Estimated for the 0.18 μm CMOS technology.

^b Estimated from the measured response in Fig. 5 of [48].

^c Information about $IIP3$ is only provided at 40 GHz in [48], which is out-of band.

C. 20-32 GHz Wideband Millimeter-Wave Mixer

Wideband mm-wave down-conversion mixer is one of the important building blocks in silicon-based receivers. This mixer should provide high conversion gain, while achieving a moderate noise figure and linearity. In addition, it should eliminate the local oscillator self-mixing problem due to the low-resistivity silicon substrate [55]. For frequencies above 20 GHz, the parasitics limit the wideband operation, and hence, reduce the conversion gain and result in to high power consumption. Solving the above challenges for a silicon-based mm-wave down-conversion mixer while reducing the power consumption is the main goal in this section.

Several techniques have been applied for down-converting narrow-band signals within the K-band [56, 57]. Sub-harmonic mixing is one of the proposed solutions to overcome the local oscillator (LO) self-mixing problem [55, 56, 57, 58] and to reduce the operating frequency of LO, hence saving the power. This technique was also employed at low-GHz frequencies [59, 60]. A frequency doubler followed by a single-ended drain mixer is applied in [56]. Due to the limited swing and low power consumption, a -11 dB conversion gain is measured at 28 GHz. Utilizing an LO with four phases and half the mixing frequency is another technique employed in [57]. In this technique, the passive sub-harmonic mixing is achieved by mixing the input signal with half the LO frequency followed by another mixing stage with the same frequency but differ by 90° phase shift. Pre- and post-amplifier stages are used to provide a conversion gain of 3.2 dB. Due to the internal parasitics and limited switch sizes, the bandwidth of the mixer was limited to 0.67 GHz to reduce the losses introduces by switches and through substrate resistance [57]. All the above techniques show that a limited operating bandwidth is the main characteristic due to internal parasitics.

To increase the bandwidth of operation at K-band, several wideband techniques

have been employed in the literature [61, 62, 63, 64, 65, 66]. Verma et al. proposed a Gilbert-cell based mixer operating at an RF signal of 19 GHz [61]. The mixer relies on two LC sections at an intermediate frequency (IF) of 2.7 GHz to provide a 1.4 GHz 3-dB IF-bandwidth. This approach relies on a narrow-band bandwidth extension technique, and therefore it is difficult to increase the IF-bandwidth. In addition, increasing the RF frequency is associated with the loss in the conversion gain because of the parasitics of the internal nodes. Lin et al. demonstrated that the conventional mixer can be used for wideband operation through increasing the power consumption (97 mW) [62]. However, the measured conversion gain shows that a flat gain is difficult to achieve for input frequencies higher than 20 GHz. This is due to the parasitics at the intermediate nodes. To overcome this limitation, Ellinger used low-Q tank circuit placed at the output of the mixer to provide the IF selection and to improve the LO to IF isolation [63]. For wideband operation, the low-Q tank reduces the conversion gain leading to a loss of 2.6 dB for 26-34 GHz frequency range and it is difficult to down-convert ultra-wide band (UWB) signals using this technique. Similar technique is applied for a resistive mixer to cover the 26.5-30 GHz frequency range [64]. Another approach is employing a passive mixer on 90-nm CMOS technology with a pi-network as the load [65]. Measurements show a conversion loss of at least 8 dB with a 9-31 GHz operating frequency range, however the 3-dB IF bandwidth is only 2 GHz. Finally, Yang et al. used a multi-layer balun in 0.13 μm CMOS technology to design a passive mixer with a conversion loss higher than 12 dB and 400 MHz IF frequency [66]. All the above technique show a trade-off between increasing the IF-bandwidth, power consumption and conversion gain (loss). Designing an active mm-wave mixer that supports a wideband flat gain for UWB signals within K-band while providing a reasonable conversion gain is an important necessity for silicon-based receivers to relax the noise figure and gain requirements of

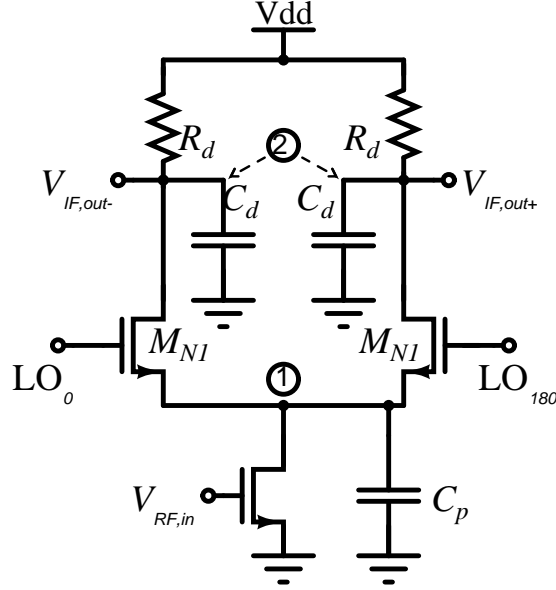


Fig. 37. The schematic of the conventional unbalanced mixer.

the low noise amplifier (LNA) and the following blocks.

In this section, a new technique for increasing the flat 3-dB IF-bandwidth of the mm-wave mixer within K-band is introduced. The approach allows increasing the 3-dB IF-bandwidth without the need for higher power consumption. In addition, a MOS-based frequency doubler with boosted output swing for higher conversion gain is used to perform for reducing the LO frequency.

1. Proposed Wideband MM-wave Mixer

a. Problem with Conventional Mixer

The conventional mixer, shown in Fig. 37, is used for wideband operation at low-GHz frequency range. However, at frequencies above 20 GHz and for wide frequency ranges, the internal parasitics limit the operation. This is because points 1 and 2 in

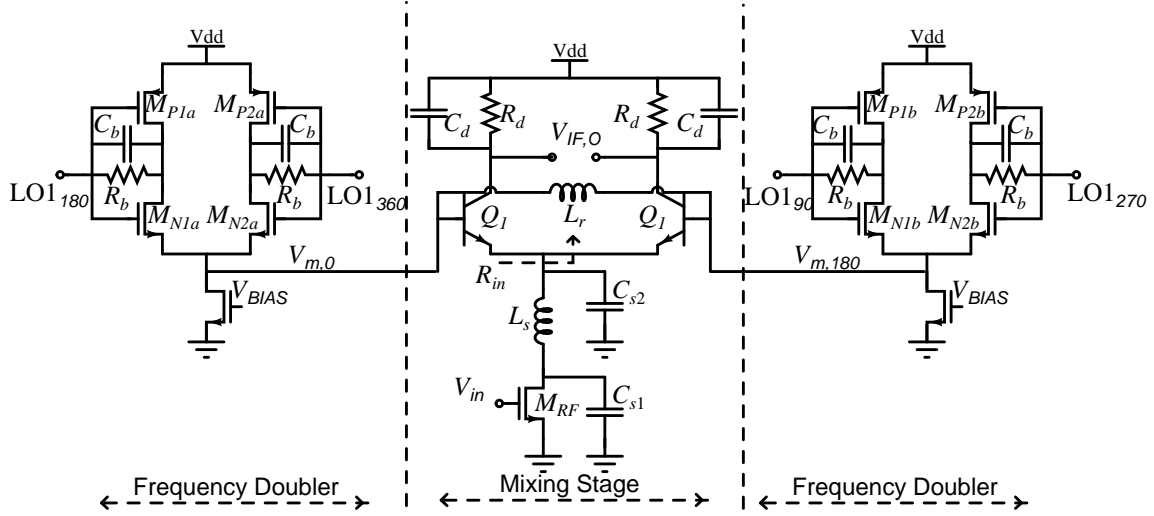


Fig. 38. The schematic of the wideband mm-wave subharmonic mixer.

Fig. 37 form a low-pass filter (LPF) for the mm-wave and IF signals, respectively. To increase the bandwidth, the size of LO switches and the value of load resistance have to be reduced to push the cut-off frequency of LPFs to higher frequencies. This comes at the cost of reducing the conversion gain and increasing the noise figure. As a result, the main limitation of bandwidth enhancement for a conventional mixer is the internal parasitics that limit the performance. To overcome this problem, a new technique is introduced to allow for wideband operation within K-band.

b. Basic Idea

Fig. 38 shows the proposed wideband mm-wave mixer. In this architecture, frequency doublers are used to avoid the LO self-mixing problem and to reduce the effective power consumption by reducing the frequency of LO to half. An LO with four phases (0° , 90° , 180° and 270°) is injected to the gate of $M_{N1,2}$, and as a result, twice of the LO frequency appears at the source of $M_{N1,2}$. Two frequency doublers are used

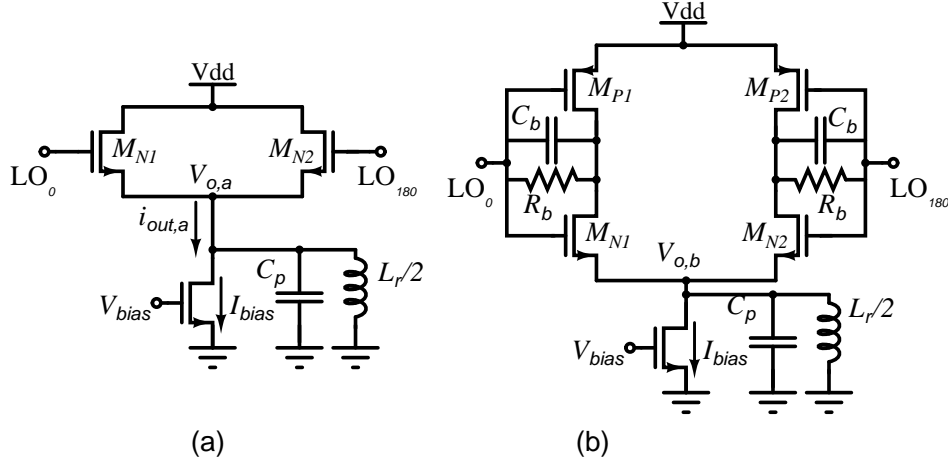


Fig. 39. Frequency doubler architectures (a) simple doubler (b) self-biased doubler with improved output swing.

to provide the out-of-phase mixing signals necessary to drive the mixer core. The inductor L_r is added to resonate with the parasitic capacitance and increase the swing at the base of the switches (Q_1), and hence increase the conversion gain and lower the noise figure of the mixer. The capacitor C_b and resistance R_b are used to increase the LO swing at sources of $M_{N1,2}$.

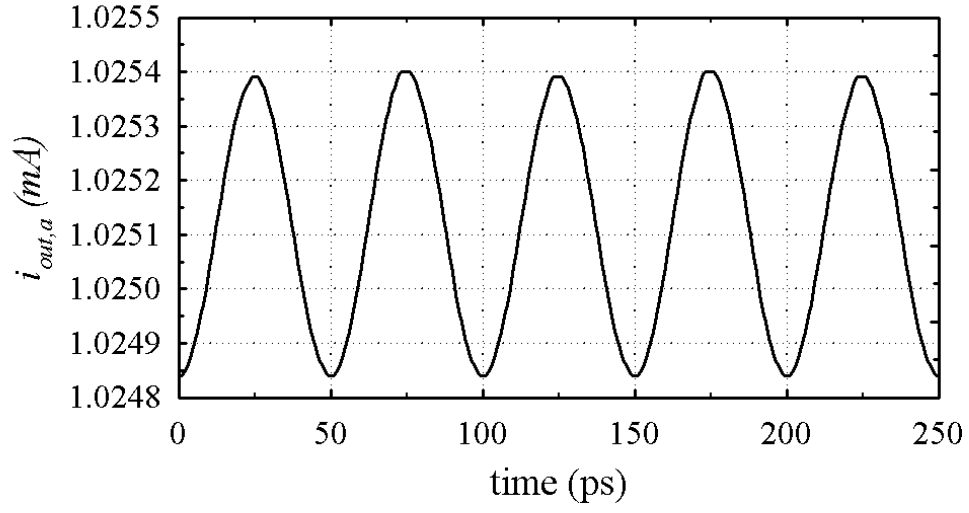
The wideband operation of the mixing stage is achieved through the introduced pi-network consisting of L_s , C_{s1} and C_{s2} . This pi-network results in peaking in the mixer transfer function aligned with the output pole ($1/(C_d R_d)$) to extend the operating bandwidth. BJT switches are used because they require an LO with lower voltage swing. All the above techniques enable the design of a wideband mm-wave mixer with a larger bandwidth and higher conversion gain while consuming lower power consumption compared to similar topologies reported in the literature. The complete analysis and design steps for the frequency doubler and the mixing stage is provided below.

Frequency Doubler: Two possible frequency doubler architectures are shown in Fig. 39. The basic operation of these frequency doublers can be summarized as follows: Two out of phase LO signals with the same frequency (f_{LO}) are applied to gates of $M_{N1,N2}$. The output is taken from sources of $M_{N1,N2}$ as demonstrated in Fig. 39 ($V_{o,a}$ in (a) and $V_{o,b}$ in (b)). Due to the differential configuration, the fundamental component of LO does not appear at the output. However because of the non-linearity of the MOSFET, twice the operating frequency ($2f_{LO}$) appears at the output. The inductor, L_r , is placed at the output to resonate with the parasitic capacitance, and thereby increasing the value of the output swing. The difference between the two architectures in Fig. 39 is the value of the output swing as demonstrated later in this section. The analysis below is initially discussed for the architecture in Fig. 39(a), then it is extended to the one in Fig. 39(b).

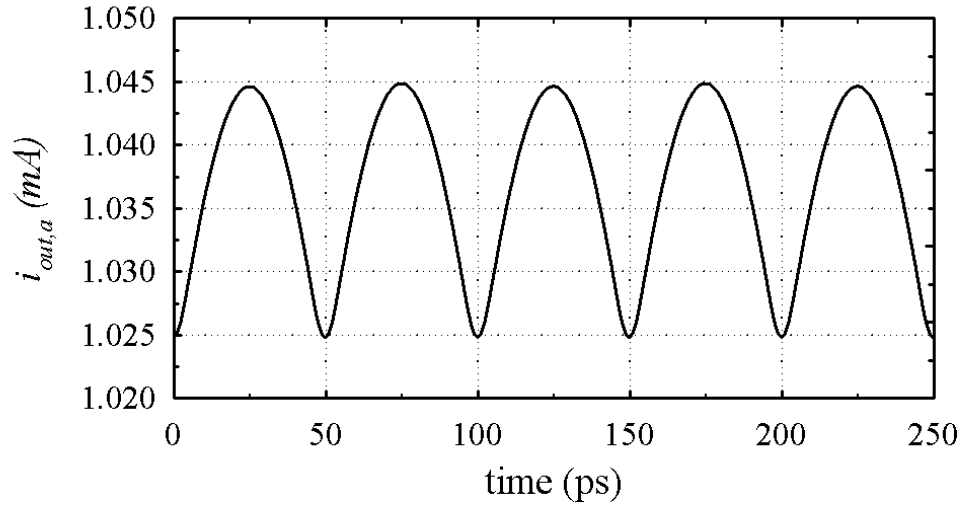
Simple Doubler: For the architecture in Fig. 39(a), two modes of operation exist depending on the amplitude of the input LO. The first mode (Mode 1) happens for small LO amplitudes such that both NMOS transistors operate all the time, and the output at $2f_{LO}$ appears due to the non-linearity of the MOS transistors. Mode 2 starts when the amplitude of the LO increases such that one of the transistors is operating while the other one is switched off. In this mode, the circuit acts as a buffer. For $LO_0 > LO_{180}$, transistor M_{N1} is on, while M_{N2} is off and vice versa. This operation is similar to a full-wave rectifier. Finally, the tank circuit consisting of C_p and L_r is tuned at $2f_{LO}$ and hence twice the operating frequency is selected at the output.

The output current in these two operating modes is simulated using Spectre ⁴ and the resultant output current $i_{out,a}$ is shown in Fig. 40. In these simulations, the

⁴Spectre 6.2, Cadence 2008



(a)



(b)

Fig. 40. Output current waveforms, $i_{out,a}$, for the two mode of operation (a) Mode 1 with $V_{LO}=50$ mV and (b) Mode 2 with $V_{LO}=500$ mV ($f_{LO}=10$ GHz, $I_{bias}=1$ mA).

effect of parasitic capacitance C_p is removed to find the shape of $i_{out,a}$. In the final implementation, an inductor $L_r/2$ is added to resonate with this capacitor at $2f_{LO}$. V_{LO} is selected to be 50 mV and 500 mV for Mode 1 and 2, respectively. As depicted, for the 50 mV case, the output current is close to a sine wave, while for an input of 500 mV the output current is close to a rectified sine wave.

For Mode 1, the amplitude at $V_{o,a}$ is found by solving the regular current equation with the restriction that the total current is I_{bias} . The resultant output amplitude at $2f_{LO}$ is given by

$$V_{o,a}(2f_{LO}) = \frac{V_{LO}^2}{2(V_{gs} - V_{th})} = \frac{V_{LO}^2}{2} \cdot \sqrt{\frac{(W/L)_{MN} \mu_n C_{ox}}{I_{bias}}}, \quad (3.29)$$

where V_{LO} is the amplitude of the input LO, $V_{gs} - V_{th}$ is the overdrive voltage, I_{bias} is the biasing current, $(W/L)_{MN}$ is the aspect ratio of the transistor $M_{N1,2}$, μ_n is the mobility, and C_{ox} is the overlap capacitance per unit area. Eq. (3.29) indicates that the output amplitude is proportional to the square of V_{LO} . In addition, reducing the gate overdrive voltage by reducing I_{bias} or increasing W/L increases the output swing. This equation is verified using schematic-level simulations and results appear in Fig. 41. The boundary limit between Mode 1 and Mode 2 is discussed later in this section. This analysis also indicates that the frequency doubler can run at low current levels as indicated by (3.29), however, the output noise is limiting the decrease of the current below a specific value. This noise is translated to a phase noise.

In the case of Mode 2, one half of the circuit is on while the other one is off. Therefore, half sine waves are introduced at the output current because the single section acts as a buffer. Using Fourier series analysis the swing at the output voltage around $2f_{LO}$ is given by

$$V_{o,a}(2f_{LO}) \approx \frac{4}{3\pi} (V_{LO} - (V_{gs} - V_{th})) \cdot \frac{g_{mn} R_{so}}{1 + g_{mn} R_{so}}, \quad (3.30)$$

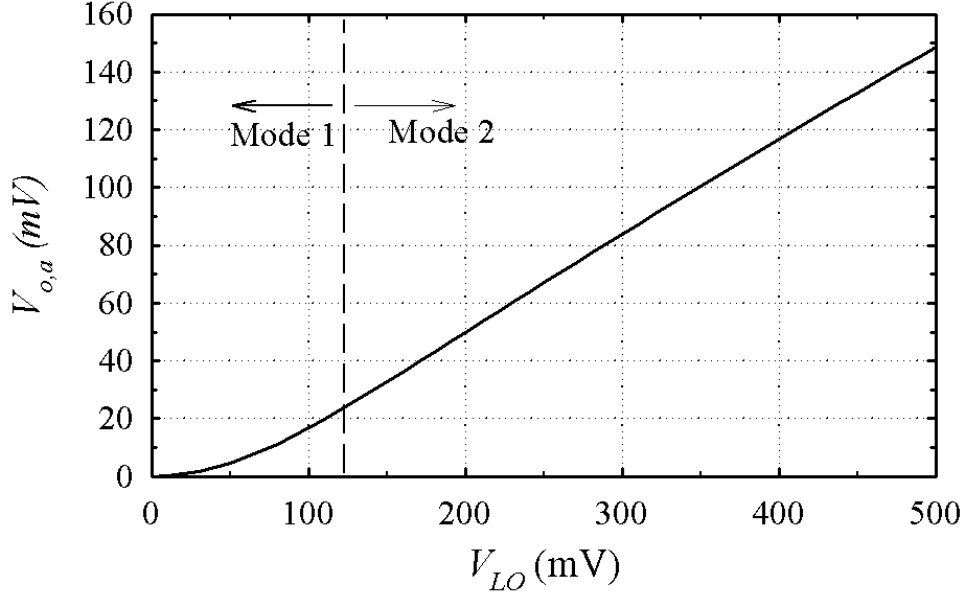


Fig. 41. Simulated output swing versus the input voltage amplitude ($f_{LO}=10$ GHz, $I_{bias}=1$ mA).

where g_{mn} is the transconductance of one of the differential pair transistors when all the value of I_{bias} flows through it, and R_{so} is the output resistance of current source. Eq. (3.30) is valid when one of the transistors is off i.e. the input voltage is high enough to drive the differential pair outside the linear region by satisfying the following condition: $V_{LO} > \sqrt{2}(V_{gs} - V_{th})$. The term $\frac{g_{mn}R_{so}}{1+g_{mn}R_{so}}$ is the buffer gain. In this case, the output amplitude increases proportionally with the amplitude of the input signals. This is verified from the schematic-level simulations as shown in Fig. 41, where the output voltage increases linearly with the value of LO amplitude. As an example, the calculated output peak amplitude using (3.30) is around 146 mVp for an input amplitude of 500 mVp, an overdrive voltage of 90 mV and a buffer gain of 0.84 ($I_{bias} = 1$ mA, $f_{LO} = 10$ GHz). This value is close to the simulated value of 149 mV, which shows the validity of the analysis.

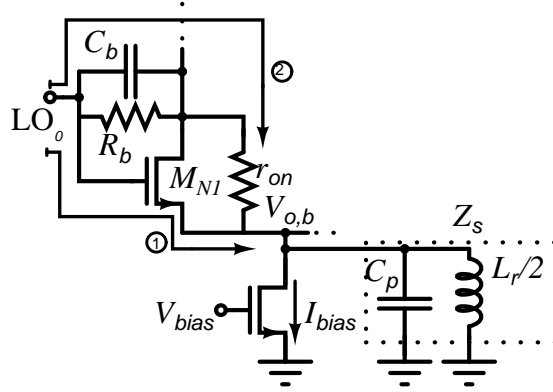


Fig. 42. Paths that contribute to the output voltage swing at $V_{o,b}$.

Doubler with Improved Output Swing: The doubler in Fig. 39(b) offers an improvement for the output swing. Yang et al. used the same architecture without the capacitor C_b to self bias the doubler [56]. However, in this implementation C_b is added to increase the output swing at $V_{o,b}$. The main reason is providing another signal path, through C_b , that increases the output swing at $V_{o,b}$ as shown in Fig. 42. The signal passing through path 2 is added coherently to the original signal passing through path 1 at the node of $V_{o,b}$. Circuit analysis shows that the output swing is given by

$$\begin{aligned}
 V_{o,b}(2f_{LO}) = & \frac{4}{3\pi} \left| \frac{g_{mn}Z_{sd}}{g_{mn}Z_{sd} + \left(1 + \frac{Z_b}{r_{on}}\right)} + \frac{sC_{gsn}Z_{sd}}{1 + \frac{g_{mn}Z_{sd}}{1 + \frac{Z_b}{r_{on}}}} \right| (V_{LO} - (V_{gs} - V_{th})), \quad (3.31) \\
 Z_b = & \frac{R_b}{1 + s \cdot C_b R_b}, \\
 Z_{sd} = & s(c_{gsn} + C_p) // sL_r // R_{so}, \\
 s = & j2\pi f_{LO},
 \end{aligned}$$

where r_{on} is the output resistance and c_{gsn} is the gate-source capacitance of $M_{N1,2}$.

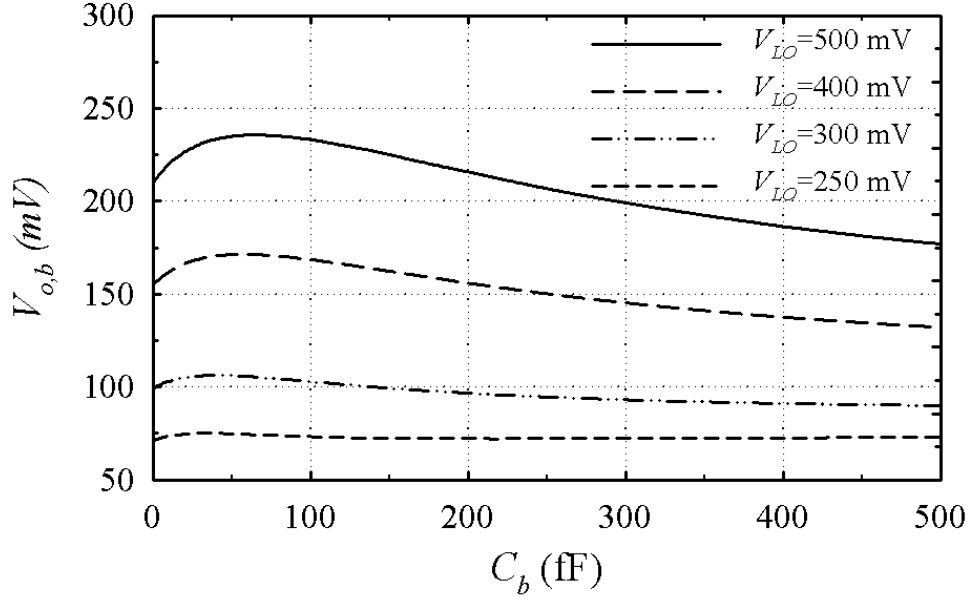


Fig. 43. The output voltage swing, $V_{o,b}$, versus C_b for different values of V_{LO} ($f_{LO}=10$ GHz, $I_{bias}=1$ mA).

Eq. (3.31) is obtained by evaluating the transfer function from the input to $V_{o,b}$ at f_{LO} . This transfer function gives the amplitude of half sine waves. The resultant value should be then multiplied by $\frac{4}{3\pi}$ to find the amplitude of the output signal at $2f_{LO}$. Fig. 43 shows the schematic-level simulated output amplitude at $2f_{LO}$ versus the value of C_b for different values of V_{LO} . As indicated for $V_{LO}=500$ mV, there is an optimum value of 60 fF for C_b resulting in a maximum output voltage amplitude of 235 mV at $2f_{LO}$ ($f_{LO}=10$ GHz, and $I_{bias}=1$ mA). Hence, the output swing increases by 60% when compared to the simple doubler case in Fig. 39. Reducing the amplitude of V_{LO} below 500 mV changes the value of optimum capacitor, which is also concluded from (3.31).

Differential LO Generation and Effect of Mismatches: The mixing stage requires a differential signal to drive BJT switches as depicted in Fig. 38. This differential

signal is generated using two frequency doublers. The inductor L_r is added across the two outputs of the doublers to resonate with the parasitic capacitance, hence increasing the output swing. These frequency doublers require a quadrature LO signal as indicated in Fig. 38. Under the ideal condition, a virtual ground appears at the middle of the inductor and two identical tank circuits appear at the output of the two doublers. These tank circuits are designed to resonate at the required mixing frequency, i.e. $2f_{LO}$.

Due to phase mismatches between the generated quadrature signals of the LO, the resulting output voltage amplitude is lower than the one estimated by (3.31). Using the equivalent circuit in Fig. 44, the differential output voltage, ΔV_m , between the two driving voltages, $V_{m,0}$ and $V_{m,180}$, is found by decomposing the half sine waveform using Fourier series analysis. Then, differential output voltage at $2f_{LO}$ is found by solving the passive circuit in Fig. 44. The outcome of this analysis is as follows

$$\begin{aligned}\Delta V_m(2f_{LO}) &= V_{m,0}(2f_{LO}) - V_{m,180}(2f_{LO}) \\ &= i_1(2f_{LO}) \cdot R \cdot \left(1 - \frac{i_1(2f_{LO})}{i_2(2f_{LO})}\right).\end{aligned}\quad (3.32)$$

where R is the resistance seen at the output, i.e. $R = \frac{1}{g_{m,N1}}$ and $g_{m,N1}$ is the transconductance of M_{N1} .

In the ideal case, there is a time shift of $\frac{1}{4f_{LO}}$ leading to $i_1(2f_{LO}) = -i_2(2f_{LO})$ and $\Delta V_{m,ideal} = 2i_1(2f_{LO})R$. Rewriting (3.32) in terms of the ideal amplitude, $\Delta V_{m,ideal}$, the differential output is written as follows

$$\begin{aligned}\frac{\Delta V_m}{\Delta V_{m,ideal}} &= \frac{1 - \frac{i_1(2f_{LO})}{i_2(2f_{LO})}}{2} \\ &= \frac{1 - \frac{i_{10}(2f_{LO})}{i_{20}(2f_{LO})} Re\{e^{j(\theta_1 - \theta_2)}\}}{2},\end{aligned}\quad (3.33)$$

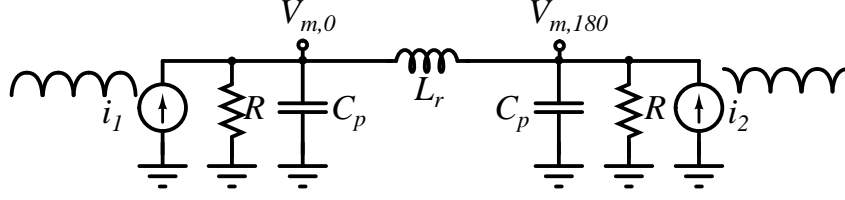


Fig. 44. Equivalent circuit of two doublers to estimate the effect of amplitude and phase mismatch.

where i_{10} and θ_1 are the amplitude and phase of i_1 , and i_{20} and θ_2 are the amplitude and phase of i_2 . In the ideal case, $i_{10} = i_{20}$ and $\theta_1 - \theta_2 = 180^\circ$. Due to amplitude and phase mismatches the differential output amplitude is changed as indicated by (3.33). Amplitude mismatches may increase or decrease the output amplitude, while phase mismatches decreases the differential output amplitude ($|Re \{e^{j(\theta_1 - \theta_2)}\}| < 1$).

This result is verified using schematic-level simulations and presented in Fig. 45 for different values of V_{LO} . In the ideal case for $V_{LO} = 500$ mV, the maximum differential amplitude is 466 mV ($I_{bias} = 1$ mA, and $f_{LO} = 10$ GHz). For a phase mismatch of $\pm 20^\circ$, ΔV_m reduces to 454 mV. This shows only a variation of 2.5% in the amplitude. Similar conclusion is observed for the different values of V_{LO} . As a result, mismatches due to process variation do not affect the functionality of this differential frequency doubler noticeably and a simple LC phase shifter can be used to generate the quadrature signal from an external differential LO signal.

Mixing Stage: The mixing stage consists of a conventional mixer as demonstrated in Fig. 38. Without the pi-network, the IF-bandwidth of the mixer is limited to a few giga-hertz at mm-wave frequencies. However, the pi-network increases the IF-bandwidth to be higher than 10 GHz. The basic idea relies on introducing a peaking in the transfer function that is aligned with the pole at the output node, $V_{IF,O}$. By

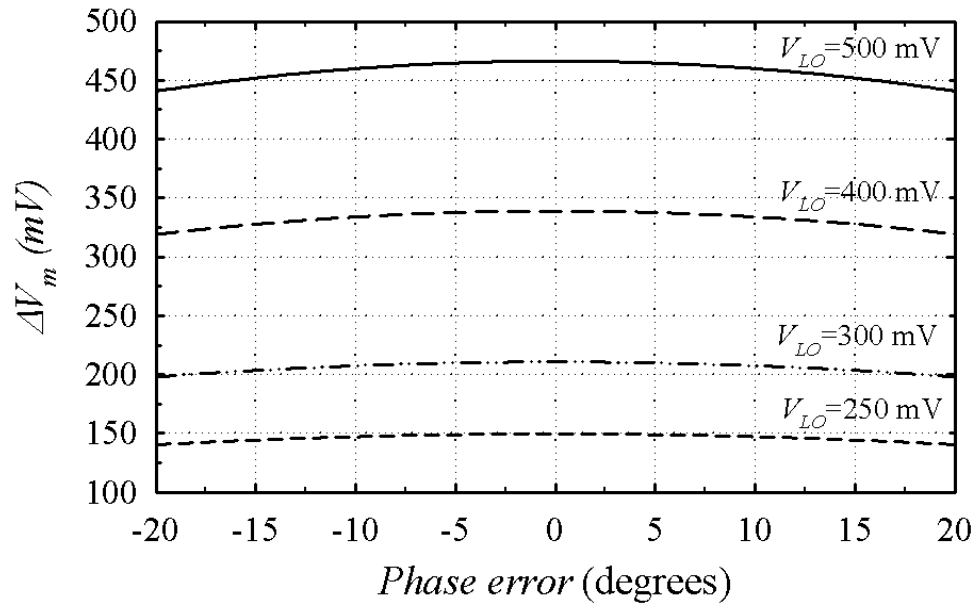


Fig. 45. Effect of phase error between quadrature signals on the output differential amplitude ΔV_m of the doubler for different values of V_{LO} ($f_{LO}=10$ GHz, $I_{bias}=1$ mA).

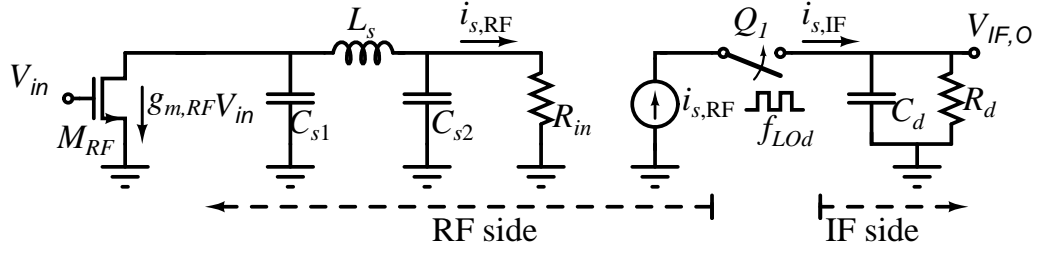


Fig. 46. Equivalent small signal model of the mixing stage.

adjusting the peaking frequency and amplitude, the bandwidth is extended to a value much higher than the case without the pi-network.

Fig. 46 shows the equivalent small-signal model of the mixing stage. Due to the mixing operation there is a signal transformation from RF to IF band by means of the switching transistor Q_1 . This is modeled by an on/off switch in Fig. 46. Based on this model, small signal analysis can be used for the signals before and after the switch, i.e. in RF and IF sections indicated in Fig. 46. The non-linear analysis should be considered for the term $\frac{i_{s,IF}}{i_{s,RF}}$, where $i_{s,RF}$ is the RF current passing through switches and $i_{s,IF}$ is the down-converted RF current to the IF frequency as shown in Fig. 46. Using Fourier series analysis, $\frac{i_{s,IF}}{i_{s,RF}}$ is found by decomposing the mixing square wave into sine waves and selecting the coefficient corresponding to IF frequency. As a result, $\frac{i_{s,IF}}{i_{s,RF}}$ is given by

$$\frac{i_{s,IF}(s_{IF})}{i_{s,RF}(s_{RF})} = \frac{2}{\pi}, \quad (3.34)$$

where $s_{RF} = j\omega_{RF}$ is the RF frequency, and $s_{IF} = j\omega_{IF}$ is the IF frequency. Assuming a low side injection of LO ($\omega_{LOd} < \omega_{RF}$), the IF frequency can be written in terms of the RF frequency as follows

$$s_{IF} = s_{RF} - j\omega_{LOd}. \quad (3.35)$$

where ω_{LOd} is the mixing frequency. Note that $\omega_{LOd} = 2\omega_{LO}$ due to the presence of frequency doublers.

The conversion gain is found by evaluating the following expression

$$\frac{V_{IF,O}(s_{IF})}{V_{in}(s_{RF})} = \frac{i_{s,IF}(s_{IF})}{i_{s,RF}(s_{RF})} \cdot \frac{i_{s,RF}(s_{RF})}{V_{in}(s_{RF})} \cdot \frac{V_{IF,O}(s_{IF})}{i_{s,IF}(s_{IF})}, \quad (3.36)$$

$\frac{i_{s,RF}(s_{RF})}{V_{in}(s_{RF})}$ and $\frac{V_{IF,O}(s_{IF})}{i_{s,IF}(s_{IF})}$ are solved analytically using small signal analysis and are given by

$$\frac{i_{s,RF}(s_{RF})}{V_{in}(s_{RF})} = \frac{g_{m,RF}}{1 + s_{RF}(C_{s1} + C_{s2})R_{in} + s_{RF}^2 L_s C_{s1} + s_{RF}^3 L_s C_{s1} C_{s2} R_{in}}, \quad (3.37)$$

$$\frac{V_{IF,O}(s_{IF})}{i_{s,IF}(s_{IF})} = \frac{R_d}{1 + s_{IF} C_d R_d}, \quad (3.38)$$

where $g_{m,RF}$ is the transconductance of the RF transistor M_{RF} , $R_{in} = \frac{1}{g_{m,Q1}}$ is the inverse of the transconductance of Q_1 , and other circuit components are as shown in Fig. 38. In the actual implementation, C_{s1} and C_{s2} include the parasitic capacitances appearing at nodes they are connected. The ratio $\frac{i_{s,RF}(s_{RF})}{V_{in}(s_{RF})}$ introduces peaking that is aligned with the IF pole in (3.38) to extend the IF-bandwidth. Eq. (3.37) can be written in terms of a single real pole and two complex poles as follows

$$\begin{aligned} \frac{i_{s,RF}(s_{RF})}{V_{in}(s_{RF})} &= \frac{g_{m,RF}}{\left(1 + \frac{s_{RF}}{\omega_1}\right) \left(1 + \frac{s_{RF}}{Q\omega_o} + \frac{s_{RF}^2}{\omega_o^2}\right)}, \\ \omega_o &\approx \frac{R_{in}^2 C_{s2}}{2L_s \sqrt{L_s C_{s1}}} \cdot \left(1 + \sqrt{1 + \frac{4L_s^2}{R_{in}^2 C_{s2}^2}}\right), \\ \omega_1 &= \frac{1}{\omega_o^2 L_s C_{s1} C_{s2} R_{in}}, \\ Q &= \frac{1}{\omega_o \left(R_{in}(C_{s1} + C_{s2}) - \frac{1}{\omega_1}\right)}. \end{aligned} \quad (3.39)$$

Eq. (3.39) highlights that the amount of peaking and 3-dB bandwidth extension depends on the value of L_s , C_{s1} , C_{s2} , and R_{in} .

Substituting (3.34), (3.35) and (3.39) into (3.36) shows that the transfer function has one real pole and two complex poles at the RF frequency side, and another real pole at the IF frequency side. The real RF pole is given by ω_1 , and two RF complex poles are defined by ω_o and Q . The real IF pole is given by $\omega_{Ld} = 1/(C_{Ld}R_{Ld})$. The two real poles reduce the gain at frequencies higher than their values, while the complex poles can be adjusted to provide peaking to reduce this decrease in the gain. This is the basic idea behind the pi-network. To achieve maximum 3-dB IF-bandwidth, both real poles should be placed at the highest possible frequency. Extending the bandwidth using this approach introduces in-band ripples. As a result, there is an optimum value for ω_o and Q to maximize the bandwidth for a given maximum in-band ripple. To find the maximum possible 3-dB bandwidth extension, (3.36)-(3.39) are solved numerically to find the value of Q and ω_o with the constraint of maximum in-band ripple.

Fig. 47 shows the simulated frequency response of the conversion gain versus IF frequency for different ripple values. In this example, ω_1 and ω_{LD} are assumed to be 40 and 5 GHz, respectively. As depicted in Fig. 47, the 3-dB bandwidth varies between 12.3 to 14.3 GHz for ripples changing from 0.1 to 1 dB, respectively. For 0.1 dB maximum in-band ripple, $Q = 4.05$ and $\omega_o = 2\pi \cdot (30.5)$ Grad/sec, while for 1 dB in-band ripple, $Q = 4.9$ and $\omega_o = 2\pi \cdot (34)$ Grad/sec. This example shows that both Q and ω_o increase as the maximum in-band ripple requirement is relaxed. Increasing Q and ω_o helps in increasing the 3-dB bandwidth as indicated in Fig. 47. This is more clarified by Fig. 48, where the term $\frac{i_{s,RF}(s_{RF})}{g_{m,RF}V_{in}(s_{RF})}$ is simulated for several values of IF in-band ripple. As depicted, increasing ω_o shifts the frequency at which $\frac{i_{s,RF}(s_{RF})}{g_{m,RF}V_{in}(s_{RF})}$ starts to increase to a higher frequency. Also, for the same ω_{Ld} and ω_1 , the increase of ω_o is associated with an increase in the value of Q , which increases in-band ripples. Hence, the highest bandwidth is achieved for 1 dB IF in-band rippled

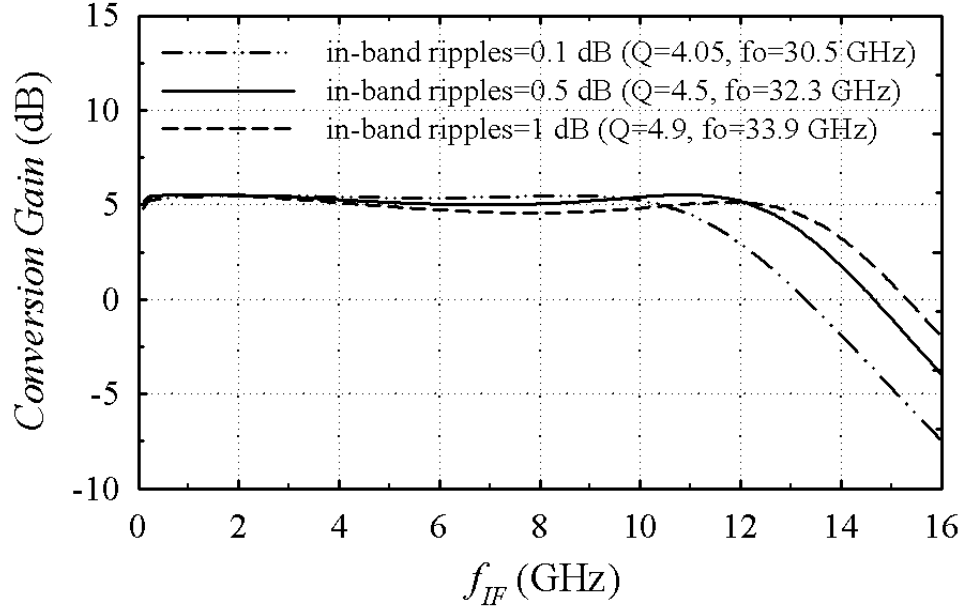


Fig. 47. Schematic-level simulation of conversion gain versus IF frequency for different values of in-band ripples.

in this example.

Another important design parameter for the pi-network is the location of ω_1 . As mentioned earlier, placing the two real poles at higher frequencies increases the bandwidth. For the IF pole at ω_{Ld} , placing the pole at a higher frequency requires decreasing the conversion gain if C_{Ld} is limited by the load capacitance. On the other hand, ω_1 should be placed at the highest possible frequency. Fig. 49(a) shows the resultant maximum 3-dB IF-bandwidth versus ω_1 for different values of ω_{Ld} and maximum in-band ripples of 0.1 and 1 dB. The maximum value of ω_1 is limited by the technology. This appears if one approximates ω_1 in (3.39) as follows

$$\omega_1 \approx \frac{1}{R_{in}C_{s2}}. \quad (3.40)$$

R_{in} in (3.40) is the inverse of the transconductance of Q_1 , and the minimum

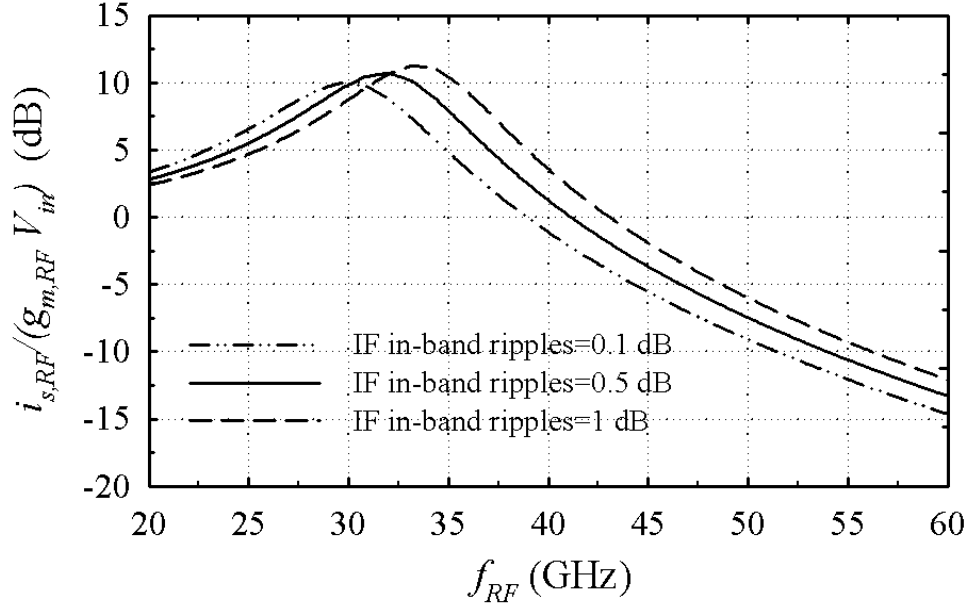


Fig. 48. Schematic-level simulation of $\frac{i_{s,RF}(s_{RF})}{g_{m,RF}V_{in}(s_{RF})}$ versus frequency for various IF in-band ripple.

value of C_{s2} is limited by base-emitter capacitance of Q_1 . Hence, the upper value for ω_1 is limited by the cut-off frequency of BJT transistor, i.e. $\omega_{1,max} = 2\pi f_{T,BJT}$. In the actual implementation, the maximum value of ω_1 is lower than the cut-off frequency because of the effect of additional parasitics. In this design, $f_{1,max} = \frac{\omega_{1,max}}{2\pi}$ is limited to 60 GHz ($f_{T,BJT} < 70$ GHz). The minimum value of ω_1 is limited by the location of the IF pole when it is transferred to the RF frequency, i.e. $\omega_{1,min} > \omega_{Ld} + \omega_{LOd}$. If ω_1 is decreased below $\omega_{Ld} + \omega_{LOd}$ the IF bandwidth will decrease significantly.

Reducing the amplitude of in-band ripples and/or ω_{Ld} reduces the resultant maximum bandwidth as shown in Fig. 49(a). Also from simulations, the increase in ω_1 is associated with an increase in ω_o and decrease in the value of Q for maximum bandwidth extension. Note that increasing ω_{Ld} by 2 GHz increases the maximum IF bandwidth by almost 3.5 GHz. The extra 1.5 GHz increase in the bandwidth is

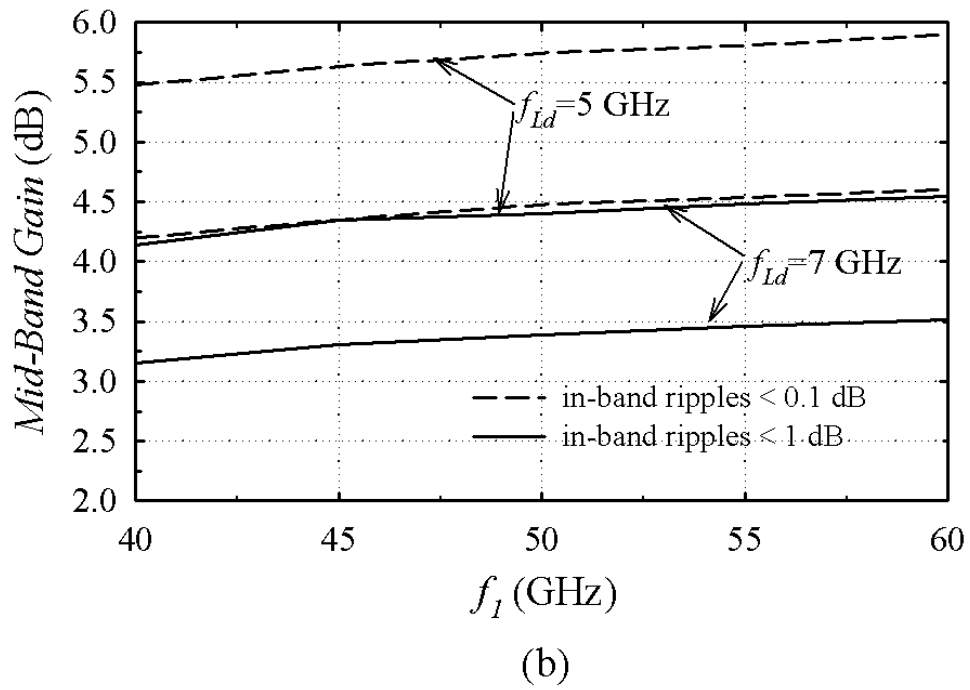
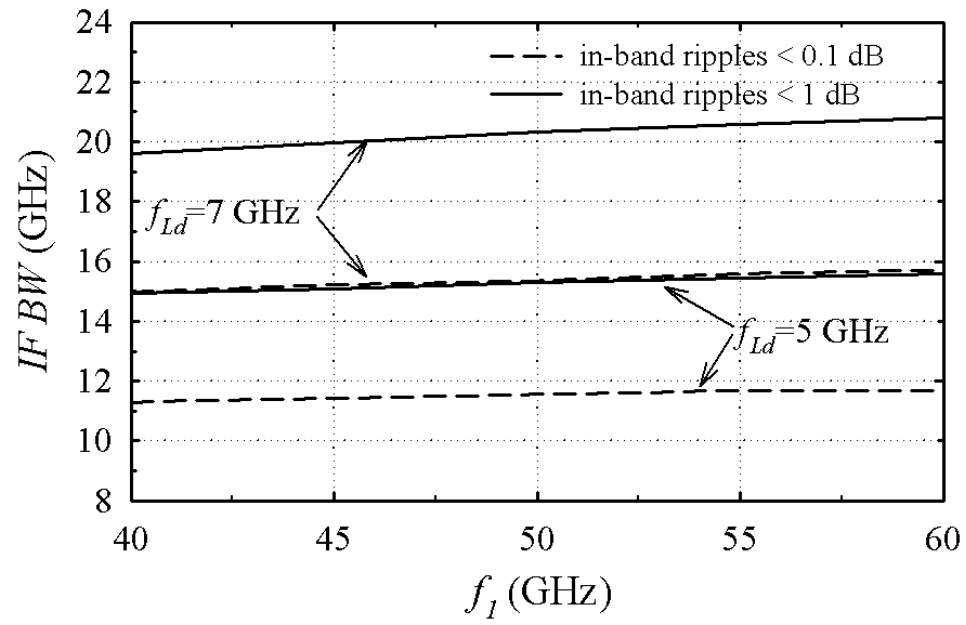


Fig. 49. (a) Maximum 3-dB IF-bandwidth and (b) conversion gain versus $f_1 = \frac{\omega_1}{2\pi}$ for different values of $f_{Ld} = \frac{\omega_{Ld}}{2\pi}$ and IF in-band ripple.

because of the drop in the value of Q as a result of having higher ω_{Ld} , i.e. in-band gain is lower. The simulated conversion gain versus ω_1 for the same test case is shown in Fig. 49(b). Also, increasing ω_1 does not change the overall IF bandwidth and conversion gain significantly.

Generally, if values of ω_{Ld} and maximum in-band ripple are known, then values for Q and ω_o that maximize the IF bandwidth are obtained numerically using (3.36) to (3.39). Values for L_s , C_{s1} , C_{s2} , and R_{in} are obtained using the expression in (3.39). It is important to note that several solutions exist to achieve the required Q and ω_o (two equations and four unknowns). The additional degree of freedom will be utilized to reduce the output noise by maximizing the value of R_{in} as will be discussed in the next section.

The above approach is verified using schematic-level simulations. In this simulation, $f_{Ld} = 5$ GHz and maximum in-band ripple lower than 0.3 dB resulting in a maximum bandwidth of 13.4 GHz for $f_1 = 40$ GHz. Fig. 50 shows the simulated conversion gain with and without the additional pi-network. Without the pi-network, C_{s1} and C_{s2} are parasitic capacitances, and $L_s = 0$. As depicted, the 3-dB bandwidth is limited to 6.2 GHz without the pi-network, and the gain is decaying with frequency. Including the pi-network increases the flat bandwidth by 115% when compared to the conventional case on the cost of decreasing the gain by almost 1 dB. Another advantage of using the pi-network is that out-of band attenuation decays faster than the conventional gain, hence providing filtering of the out-of-band signals.

2. Noise Analysis

In this section, the noise figure analysis of the proposed subharmonic mixer is demonstrated. The noise due to the RF transistor, M_{RF} , switching transistors, Q_1 , and load resistance R_L is considered in this analysis.

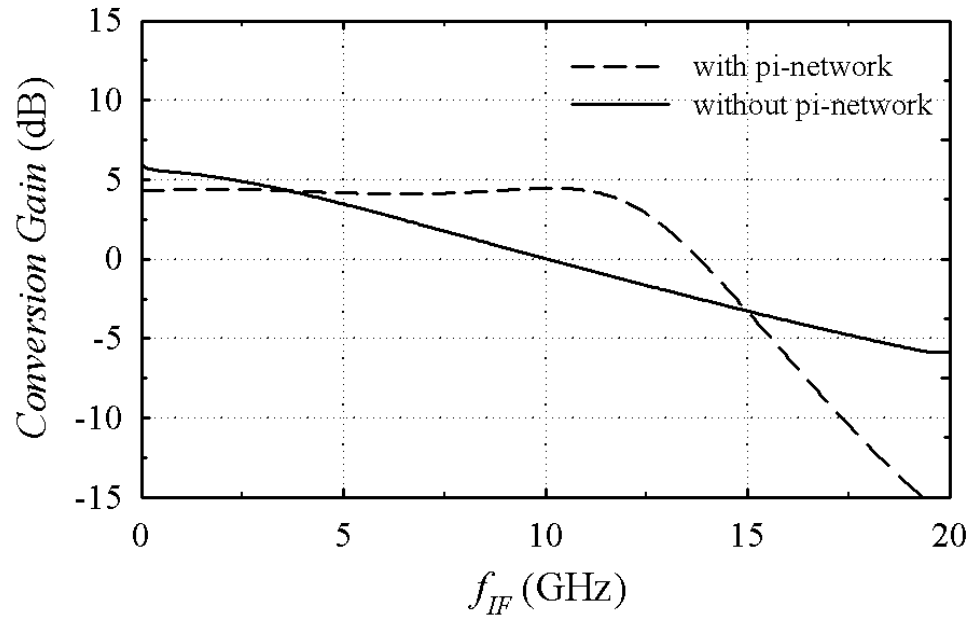


Fig. 50. Schematic-level simulation of conversion gain versus IF frequency with and without the pi-network.

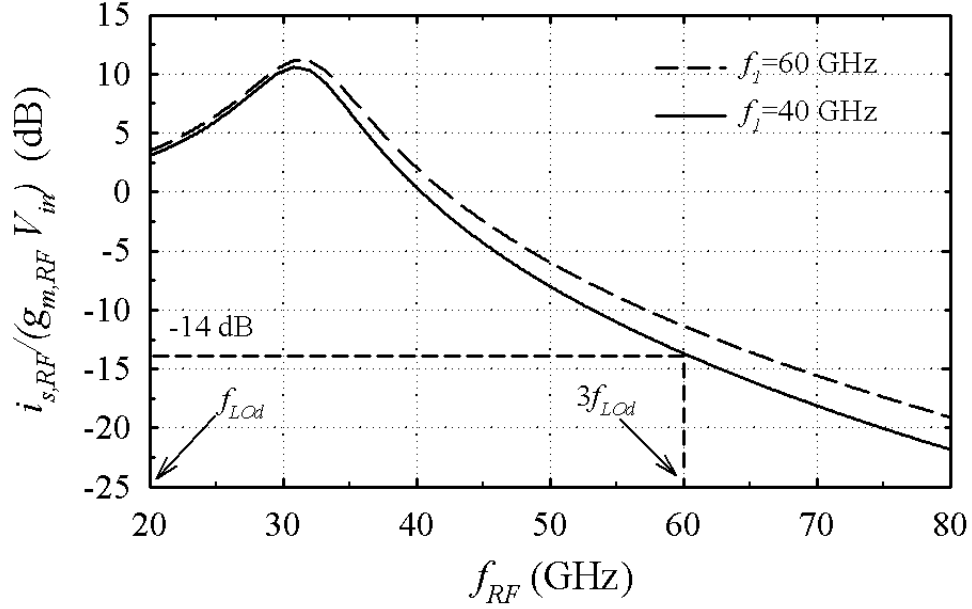


Fig. 51. Schematic-level simulation of $\frac{i_{s,RF}(s_{RF})}{V_{in}(s_{RF})}$ for f_1 of 40 and 60 GHz.

a. RF Transistor Noise

The thermal noise of the transconductance appears at the output IF frequency. Due to the mixing operation, noise around ω_{LOd} , $3\omega_{LOd}$, $5\omega_{LOd}$, .. etc. fold back into the baseband frequency of interest [32]. Because of the limited bandwidth of the pi-network, the noise around frequencies of odd multiples of ω_{LOd} are attenuated. To attenuate the noise further, capacitor C_{s2} is increased to reduce the value of ω_1 such that the folded noise at odd multiples of ω_{LOd} is attenuated. This conclusion is verified using schematic-level simulations of $\frac{i_{s,RF}(s_{RF})}{V_{in}(s_{RF})}$ for f_1 of 40 and 60 GHz and the results are shown in Fig. 51, where the noise appearing at $3f_{LOd}$ is attenuated by 14 dB for $f_1 = 40$ GHz. Flicker noise does not appear at the output because it is upconverted around ω_{LOd} after the mixing operation [32].

Based on the above discussion, the folded noise due to the mixing operation at

ω_{LOd} , $3\omega_{LOd}$, $5\omega_{LOd}$, .. etc. is neglected. Hence, the input referred and output noise voltage spectral densities, $\frac{\overline{v_{i,nRF}^2}}{\Delta f}$ and $\frac{\overline{v_{o,nRF}^2}}{\Delta f}$, due to the RF transistor are given by

$$\begin{aligned}\frac{\overline{v_{i,nRF}^2}}{\Delta f}(\omega_{RF}) &= \frac{4kT\gamma}{g_{m,RF}} \cdot \left(1 + \left|\frac{V_{in}(s_{RF})}{V_{in}(s_{LOd} - s_{IF})}\right|^2\right), \\ \frac{\overline{v_{o,nRF}^2}}{\Delta f}(\omega_{IF}) &= \frac{\overline{v_{i,nRF}^2}}{\Delta f}(\omega_{RF}) \cdot \left|\frac{V_{IF,O}(s_{IF})}{V_{in}(s_{RF})}\right|^2.\end{aligned}\quad (3.41)$$

where k is Boltzmann constant, T is the temperature in Kelvin, and γ is the channel noise factor. The first term in (3.41) is due to down-converted upper side-band noise (above LO frequency), while second term is due to the lower side-band noise (below LO frequency). Eq. (3.41) also indicates that increasing $g_{m,RF}$ increases the output noise, however, the input referred noise is decreased.

b. Load Resistance Noise

The load noise appears at the output directly. In this design, a resistive load is used for the mixer. Since the output pole is lower than the operating bandwidth, the thermal noise of the resistance is attenuated at frequencies above the output pole, ω_{Ld} . Hence, the input referred and output noise voltage spectral densities due to R_{Ld} are given by

$$\begin{aligned}\frac{\overline{v_{i,nRLD}^2}}{\Delta f} &= \frac{8kTR_{Ld}}{1 + (\omega C_{Ld}R_{Ld})^2} \left|\frac{V_{IF,O}(s_{IF})}{V_{in}(s_{RF})}\right|^2, \\ \frac{\overline{v_{o,nRLD}^2}}{\Delta f} &= \frac{8kTR_{Ld}}{1 + (\omega C_{Ld}R_{Ld})^2}.\end{aligned}\quad (3.42)$$

Eq. (3.42) points out that the contribution of R_{Ld} to the input referred noise is lower at higher frequencies because the noise is getting attenuated by the output pole, and the overall gain, $\left|\frac{V_{IF,O}(s_{IF})}{V_{in}(s_{RF})}\right|$, across the entire bandwidth is constant. This is clarified by noting that the pi-network introduces a peaking that is aligned with

the output pole, hence providing an almost constant gain across the entire band.

c. Switching Transistors Noise

The noise in switching transistors is due to base and collector noise currents, and base resistance noise voltage. For BJT, the base resistance noise voltage, and the base and collector noise currents are given by

$$\frac{\overline{v_{n,rb}^2}}{\Delta f} = 4kTr_{b,Q1}, \quad (3.43)$$

$$\frac{\overline{i_{n,b}^2}}{\Delta f} = 2qI_{b,Q1} = \frac{2q}{\beta}g_{m,Q1}V_T = \frac{2kT}{\beta}g_{m,Q1}, \quad (3.44)$$

$$\frac{\overline{i_{n,c}^2}}{\Delta f} = 2qI_{c,Q1} = 2qg_{m,Q1}V_T = 2kTg_{m,Q1}, \quad (3.45)$$

where $V_T = kT/q$ is the thermal voltage, q is the electron charge constant, and β is the current gain. $g_{m,Q1}$, $I_{b,Q1}$ and $I_{c,Q1}$ are the transconductance, base and collector currents of $Q1$, respectively.

The noise appearing at the output due to the switching transistors comes from two major mechanisms. The first one appears when both switches are on and the differential LO amplitude is crossing the zero point. Similar approach reported in [32] is used to find the amount of output noise in case a BJT is used instead of a MOS transistor. Assuming an LO signal with a sine wave shape, the input referred and output noise spectral densities are given by

$$\begin{aligned} \frac{\overline{v_{i,ns w1}^2}}{\Delta f} &= \frac{2kT \cdot I_{c,Q1}}{\pi A_{LOd}} \cdot \frac{R_{Ld}^2}{1 + (\omega C_{Ld} R_{Ld})^2} / \left| \frac{V_{IF,O}(s_{IF})}{V_{in}(s_{RF})} \right|^2, \\ \frac{\overline{v_{o,ns w1}^2}}{\Delta f} &= \frac{2kT \cdot I_{c,Q1}}{\pi A_{LOd}} \cdot \frac{R_{Ld}^2}{1 + (\omega C_{Ld} R_{Ld})^2}, \end{aligned} \quad (3.46)$$

where A_{LOd} is the amplitude of the sine wave driving the switches. The calculated output noise in (3.46) is due to the collector noise current only. Base noise current

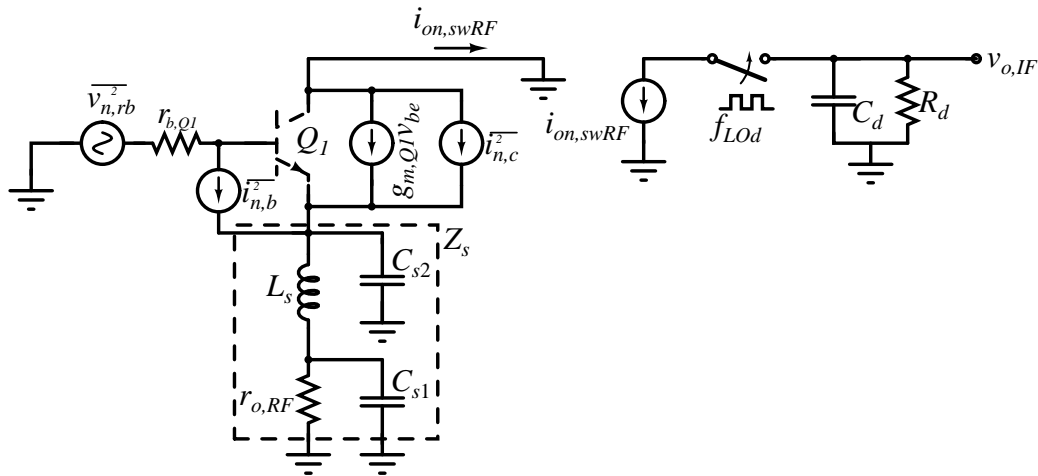


Fig. 52. Noise sources of switching transistor, Q_1 , when one switch is on.

does not appear at the differential output because it is injected into the common node of switches. Hence, it appears at both outputs with the same amount, and it is differentially removed.

The second mechanism appears only at mm-wave frequencies. This is because under hard switching condition, the transistor Q_1 is not degenerated with a high impedance when one of the switching transistors is on while the other one is off. Hence, the noise due to Q_1 appears at the output and the overall output noise is increased. This situation is not the case for low giga-hertz frequencies, because the effect of parasitic capacitance at the emitter of Q_1 can be neglected, and a large degeneration resistance at the emitter of Q_1 prevents the noise from appearing at the output.

Fig. 52 shows the equivalent circuit used to find the contribution of Q_1 to the output noise. In this case, Q_1 is degenerated with the impedance consisting of L_s , C_{s1} , C_{s2} , and $r_{o,RF}$ (output resistance of RF transistor). Since the circuit switches on and off periodically with a duty cycle of 50%, the output noise is convoluted with

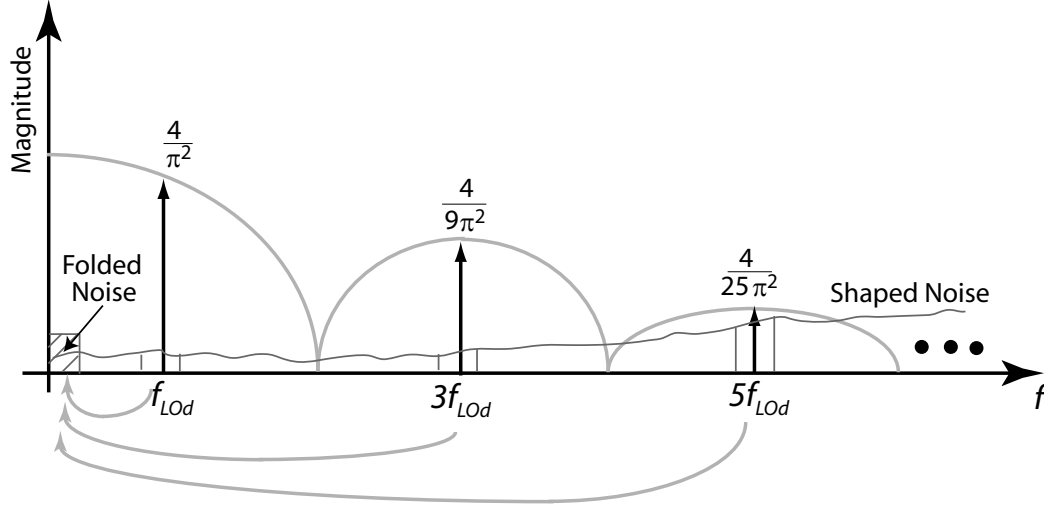


Fig. 53. Demonstration of the folded noise of switching transistors to baseband when one of them is on while the other one is off.

delta functions appearing at ω_{LOd} , $3\omega_{LOd}$, $5\omega_{LOd}$, \dots , and the noise appearing at these frequencies is folded back to baseband. The amplitude of these delta functions is shown in Fig. 53.

Superposition is used to find the noise contribution of each noise source at the output IF frequency independently. The RF noise current, $i_{on,swRF}$ in Fig. 52, is initially found by solving the equivalent noise small signal model. Then, the down-converted noise is obtained by convolving $i_{on,swRF}$ and the delta functions appearing due to the switching in the frequency domain. This approach results in the down-converted noise in the IF bandwidth. In this analysis, both the upper side and the lower side noise should be considered in the final expression.

The output noise voltage due to collector noise current is given by

$$\frac{\overline{v_{o,nsww2,ic}^2}}{\Delta f}(\omega_{IF}) = 2 \sum_{n=-\infty, \text{nodd}}^{n=\infty} \frac{8kTg_{m,Q1}}{\pi^2 n^2} \cdot \frac{1}{|1 + g_{m,Q1}Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2} \cdot \frac{R_{Ld}^2}{1 + (\omega_{IF}C_{Ld}R_{Ld})^2}, \quad (3.47)$$

where Z_s is as shown in Fig. 52. The multiplication by two that appears before the summation in (3.47) is because of two switching transistors, each is operating in a different time window. The term $\frac{4}{\pi^2 n^2}$ appears due to the effect of the delta functions in Fig. 53. The contribution of the upper and lower side noise is considered in (3.47) by defining limits of the summation from minus to plus infinity.

Similar analysis is performed to find the contribution of base current noise and base resistance noise, and the resultant output noise voltages are given by

$$\frac{\overline{v_{o,nsww2,ib}^2}}{\Delta f}(\omega_{IF}) = 2 \sum_{n=-\infty, \text{nodd}}^{n=\infty} \frac{8kTg_{m,Q1}}{\pi^2 n^2} \cdot \frac{\frac{g_{m,Q1}^2}{\beta} |Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2}{|1 + g_{m,Q1}Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2} \cdot \frac{R_{Ld}^2}{1 + (\omega_{IF}C_{Ld}R_{Ld})^2}, \quad (3.48)$$

$$\frac{\overline{v_{o,nsww2,rb}^2}}{\Delta f}(\omega_{IF}) = 2 \sum_{n=-\infty, \text{nodd}}^{n=\infty} \frac{8kTg_{m,Q1}}{\pi^2 n^2} \cdot \frac{2r_{b,Q1}g_{m,Q1}^2}{|1 + g_{m,Q1}Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2} \cdot \frac{R_{Ld}^2}{1 + (\omega_{IF}C_{Ld}R_{Ld})^2}. \quad (3.49)$$

Finally, the total output noise due to the second mechanism is found by summing (3.47) to (3.49) yielding the result in (3.50).

$$\frac{\overline{v_{o,nsww2}^2}}{\Delta f}(\omega_{IF}) = 2 \sum_{n=-\infty, \text{nodd}}^{n=\infty} \frac{8kTg_{m,Q1}}{\pi^2 n^2} \cdot \frac{1 + \frac{g_{m,Q1}^2}{\beta} |Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2 + 2r_{b,Q1}g_{m,Q1}^2}{|1 + g_{m,Q1}Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2} \cdot \frac{R_{Ld}^2}{1 + (\omega_{IF}C_{Ld}R_{Ld})^2}. \quad (3.50)$$

Eqs. (3.46) and (3.50) show that the output noise reduces as the transconductance

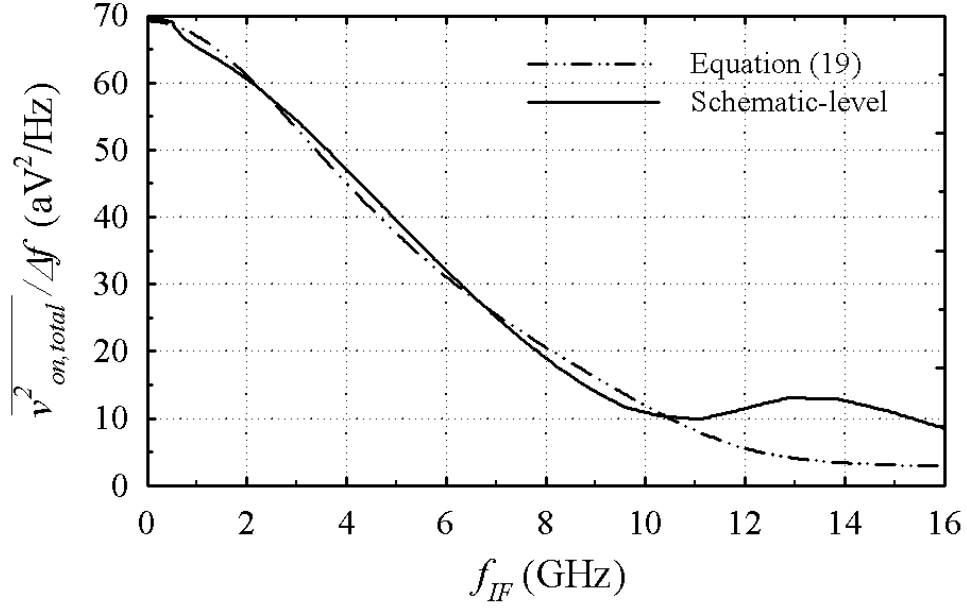


Fig. 54. Schematic-level simulated and predicted output noise voltage spectral density.

value of Q_1 decreases (R_{in} is increased). This constraint can be used as an additional requirement to determine the value of the pi-network parameters discussed in the previous section.

d. Total Input Noise

The total output referred noise is found by summing all the noise terms in (3.41), (3.42), (3.46), and (3.50). The resultant total input referred noise is given by (3.51).

$$\begin{aligned} \frac{\overline{v_{on,total}^2}}{\Delta f}(\omega_{IF}) &= \frac{4kT}{g_{m,RF}} \cdot \left| \frac{V_{IF,O}(s_{IF})}{V_{in}(s_{RF})} \right|^2 + \frac{2kTR_{Ld}^2}{1 + (\omega_{IF}C_{Ld}R_{Ld})^2} \cdot \\ &\left(\frac{4}{R_{Ld}} + \frac{I_{c,Q1}}{\pi A_{LOd}} + \sum_{n=-\infty}^{n=\infty} \frac{8g_{m,Q1}}{\pi^2 n^2} \cdot \frac{1 + \frac{g_{m,Q1}^2}{\beta} |Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2 + 2r_{b,Q1}g_{m,Q1}^2}{|1 + g_{m,Q1}Z_s(\omega_{RF} - n \cdot \omega_{LOd})|^2} \right). \end{aligned} \quad (3.51)$$

The noise analysis presented in this section is verified using schematic-level simulations. Fig. 54 shows the schematic-level simulated output noise voltage spectral

density versus the IF frequency and the total output noise predicted by (3.51). As indicated, the theory matches closely the simulation results up to 11 GHz. The discrepancy at frequencies higher than the operating IF bandwidth is because of the approximations considered in deriving (3.51). The noise below 10 GHz is mainly due to the noise generated by switches. This analysis proves that the noise of switches due to the second mechanism is an important factor for active mixers operating at mm-wave frequencies.

3. Simulation and Experimental Results

The wideband mm-wave mixer is fabricated using $0.18\ \mu\text{m}$ BiCMOS technology provided by Jazz Semiconductor. The die micrograph is shown in Fig. 55, where the total area is $0.19\ \text{mm}^2$, excluding pads and output buffer. The mm-wave input, output, LO signal, and DC biasing signals are applied and monitored using on-wafer probing to reduce the losses and mismatches introduced by the measurement setup. Ground-Signal-Ground (GSG) probes are used to apply the input signal, and Ground-Signal-Ground-Signal-Ground (GSGSG) differential probes are used to derive the LO signal and to measure the IF signal at the output. An 8 pin DC probe is used to apply the required DC biasings. The external LO is running at 10 GHz (effective mixing frequency of 20 GHz) with an input power of 5 dBm. The effect of the output buffer is de-embedded from the mixer+buffer measurements. The buffer is added at the output of the mixer to drive the $50\ \Omega$ input impedance of the network analyzer.

The conversion gain is measured by applying an input signal using Agilent N5230A network analyzer and measuring the output using the spectrum analyzer. The simulated and measured conversion gain after de-embedding the buffer and cable loss effects are shown in Fig. 56. The measured conversion gain is 3 dB with a 3-dB IF bandwidth of 12 GHz. The post-layout simulated conversion gain is 4 dB

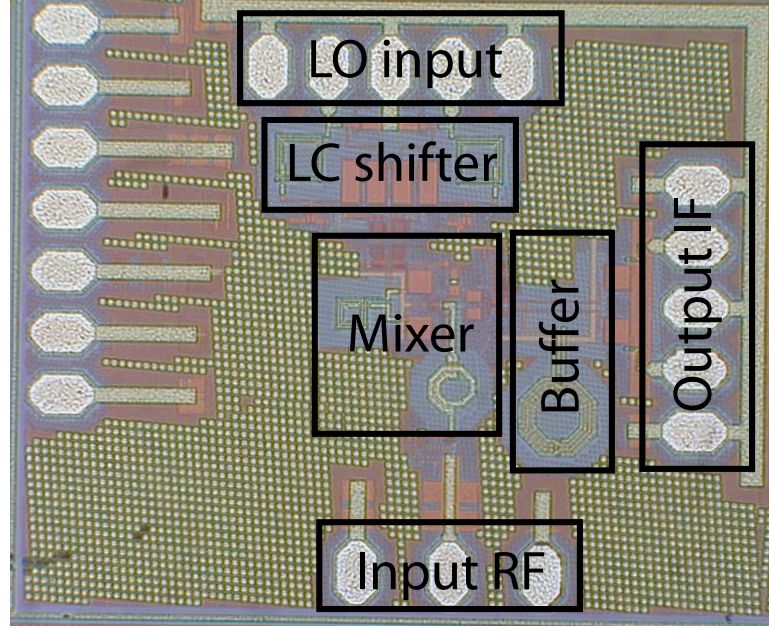


Fig. 55. Die-photo of the mm-mixer with an area of 0.19 mm^2 (pads and buffer are not included).

with a bandwidth of 13 GHz. The difference between the simulated bandwidth and measured one could be due to the non-accurate models of the transistors that may lead to extra capacitance, and/or the effect of process variation.

The measured noise figure versus the IF frequency is shown in Fig. 57, where the noise figure varies from 10.5 to 13.5 dB. As indicated, the noise figure initially decreases as the IF frequency increases. This is because the pi-network impedance increases with the RF frequency to provide the required peaking. As a result, the noise contribution of the switches is reduced.

A two-tone IIP_3 measurement is performed for the mixer and the results are shown in Fig. 58 for the 20-32 GHz frequency range. The two tones are applied with the same amplitude and a frequency offset of 50 MHz. The measured IIP_3 changes from 0.5 to 2.6 dBm across the entire frequency range. The core cell of the

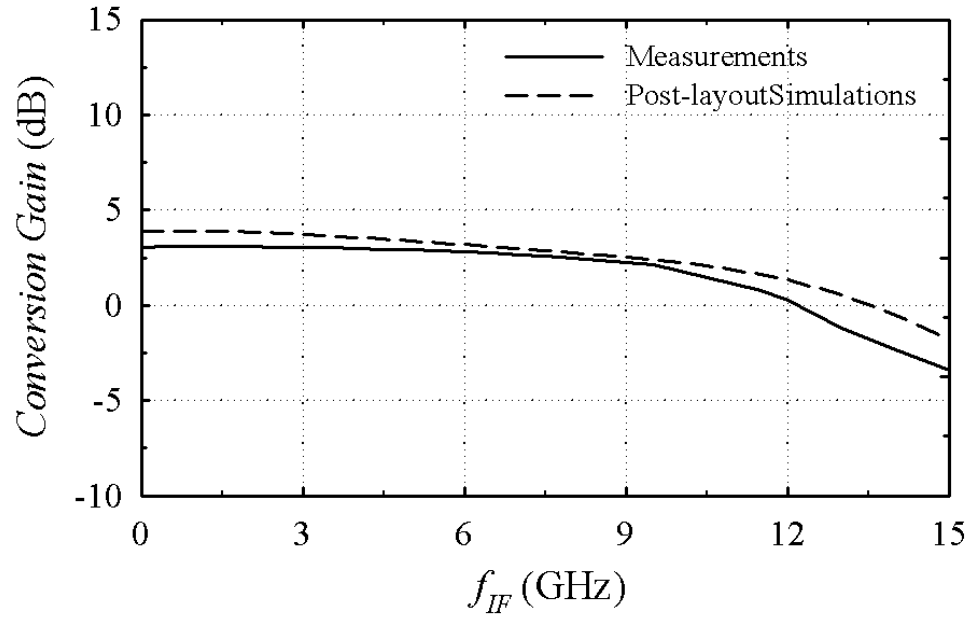


Fig. 56. Measured and simulated conversion gain of the proposed mm-wave mixer.

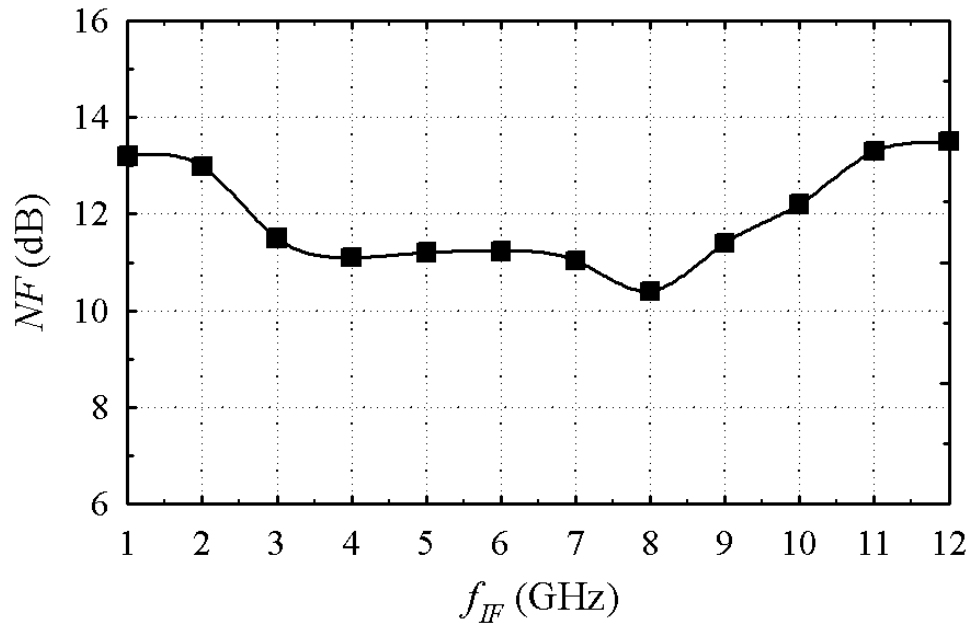


Fig. 57. Measured noise figure of the proposed mm-wave mixer.

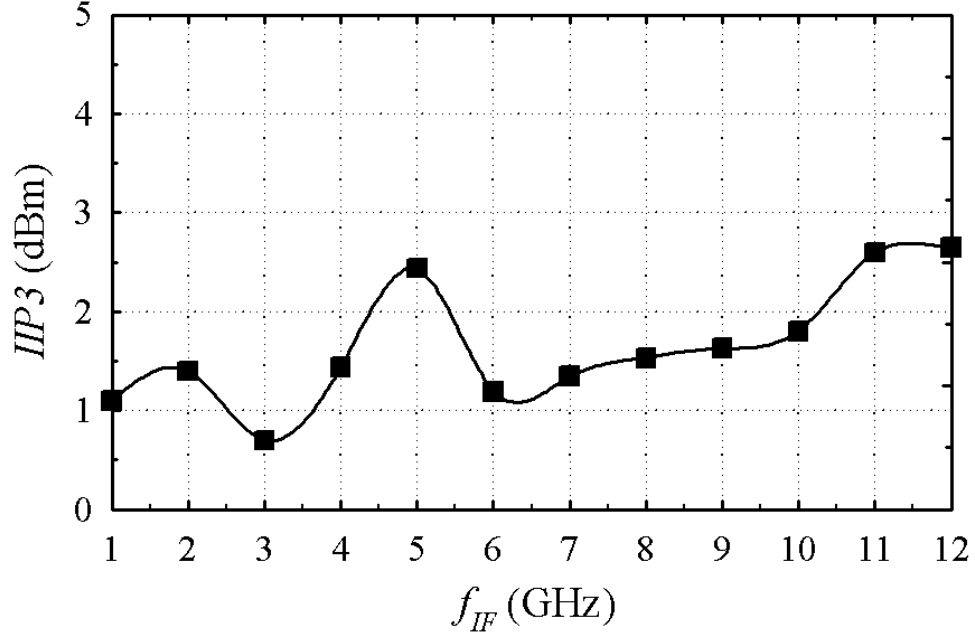


Fig. 58. Measured IIP_3 of the proposed mm-wave mixer.

mm-wave mixer consumes 7 mA from a 1.8 V supply, and each doubler consume 1.5 mA from the same supply. The performance of the proposed wideband mm-wave mixer and comparison with other existing mixer around the same frequency range are summarized in Table VIII. The proposed mixer achieves the widest IF bandwidth, and comparable NF and IIP_3 compared to state-of-the-art.

Table VIII. Performance summary of the proposed mm-wave mixer and comparison with the existing work.

Ref.	RF Freq. Range (GHz)	IF BW (GHz)	SSB NF (dB)	Gain (dB)	IIP3 (dBm)	P_{DC} (mW)	P_{LO} (dBm)	f_T (GHz)	Active Area (mm ²)	Technology
[61]	18.3-19.7	1.4	9	1	-2	6.8	-1	90 ^a	0.53	0.13 μ m CMOS
[62]	10 - 22 ^b	NA	16.4	12 ^b @ 15 GHz	(-0.2)-4.5	97	5	76	0.25	0.13 μ m CMOS
[63]	26 - 34	0.5 ^c	13.5	-2.6	0.5	20	5	160	0.2	90 nm SOI
[64]	26.5 - 30	3.5	11.4	-10.3	12.7	0	5 ^d	160	0.12	90 nm SOI
[65]	9 - 31	2	NA	-8	3	0	9.7	170	0.94 ^e	90 nm CMOS
[66]	16 - 46	0.4	17.4	-13	14	0	11	55	0.24 ^e	0.18 μ m CMOS
This work	20 - 32	12	13.5-10.5	3	0.5-2.6	18	5	70	0.19	0.18 μ m BiCMOS

^a Estimated for 0.13 μ m CMOS technology.

^b Estimated from the measured response in Fig. 3 of [62].

^c Estimated from the parameters values of the tank load in Fig. 1 of [63].

^d LO power at which NF is measured.

^e Area including pads.

D. IF amplifier and Switchable Harmonic Mixer

1. Switchable Harmonic Mixer

The switchable harmonic mixer is the main block of the proposed receiver. Fig. 59 shows the implementation of the switchable harmonic mixer, which is similar to an implementation in [67] that is used in a highly linear transmitter. The mixer in Fig. 59 consists of three Gilbert-cell mixers each driven with a different LO signal. According to Table VI, the middle mixer provides a conversion gain $\sqrt{2}$ times higher than the other two mixers. This is achieved by scaling the transconductance value of M_2 to a value of $\sqrt{2}$ times higher than the transconductance value of M_1 and M_3 . The value of transconductance can be scaled by increasing the current through the biasing transistor, M_{B2} , by two, or increasing the size of M_2 by the same ratio when compared to M_1 and M_3 . In this implementation, the first approach is used to avoid increasing the size of M_2 to reduce the parasitic capacitances that attenuate the signal at higher frequencies. NMOS RF transistors are chosen for the RF input stage to minimize the loading on the preceding stage in the receiver. Also they have the advantage of better linearity compared to bipolar junction transistors which need some linearization technique and make the matching between the three mixing cells a harder design problem. The biasing transistors M_{B1} , M_{B2} , and M_{B3} are designed to be large enough to reduce the overdrive voltage for higher voltage headroom, and to help increase the matching between the devices. Bipolar junction transistors are used for the LO input stage to minimize the flicker noise of the switches. In addition, bipolar transistor require small LO signal amplitude (≈ 200 mV) for switching. The number of base fingers of the bipolar transistor is increased to reduce its generated output noise.

To overcome the tradeoff between increasing the conversion gain, by increasing

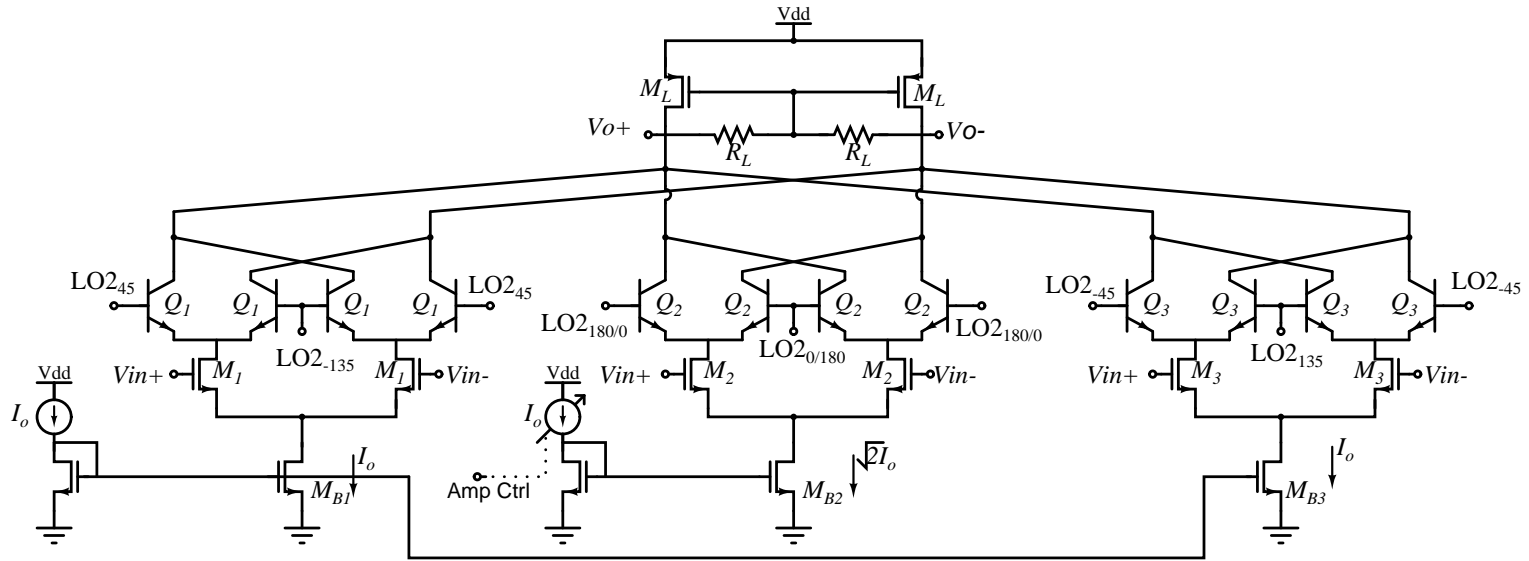


Fig. 59. Architecture of the switchable harmonic mixer. The selection of either the fundamental or the third order harmonic component is achieved by changing the phase of middle mixing stage.

the current, and the available headroom, PMOS current steering technique is used as shown in Fig. 59. Current steering is implemented through the transistor M_L and resistor R_L . This is because the output DC voltage is determined by the gate overdrive voltage of PMOS devices. During AC operation, the passive resistor, R_L , appears and controls the conversion gain. This technique does not require a common mode feedback circuit as R_L provides a local feedback to stabilize the output DC voltage. The area of PMOS transistors is increased to minimize their flicker noise contribution. In this implementation, the flicker noise that appears at the output is mainly due to the PMOS load. Additionally, slight degradation in the linearity is observed due to the nonlinear output resistance of PMOS transistors.

The LO signals are driven from the same source, and they have the same frequency of 3.5 GHz but are different in phase, according to Table VI. This mixer provides down-conversion of the signals at 3.5 and 10.5 GHz, which are the IF frequencies of 24 and 31 GHz frequency bands. The fundamental (3.5 GHz)/third order harmonic (10.5 GHz) selection is achieved by controlling the phase of the input LO signal of the middle mixer in Fig. 59. If the phase of LO signal is zero degree, then the fundamental component is selected while the third harmonic component is rejected. On the other hand if the phase is 180 degrees, then the third harmonic component is selected and the fundamental one is rejected. This approach enables the use of a single switch to control the required band selection.

2. Poly-Phase Shifter

A two-stage poly-phase shifter, shown in Fig. 60, is used to generate the required $\pm 45^\circ$ phase shifts. Two-stage poly-phase shifter is used to provide a more precise phase shift with the drawback of 3 dB loss. Simulations across the process corners show a precise phase shift of 90° between nodes $LO2_{45}$ and $LO2_{-45}$ in Fig. 60 as

long as nodes 1 and 2 are not loaded. The $0^\circ/180^\circ$ phase shifts are taken from main LO input signal (LO_{main+} , LO_{main-}) to reduce the loading on nodes 1 and 2, and they are injected to a multiplexer. The control line of this multiplexer determines the desired band. Due to the additional multiplexer, the phase shift is not $0^\circ/180^\circ$, and therefore an additional RC phase shifter, shown in Fig. 61, is added to reduce the amplitude of LO2, such that the driving amplitude of the switches is the same for the three mixers for better matching. The capacitor, C_o is chosen to be double the value of the capacitor, C_p of the poly-phase filter, to have almost same amplitude for all LO output signals. The resistance R_o is externally controlled through the transistor M_o to account for the phase mismatch between $LO2_0$ and $LO2_{45}/LO3_{-45}$ that are generated due to process variations. This control, $V_{control}$ in Fig. 61, can be used in an automatic tuning scheme to provide the necessary phase correction and hence increase the amount of rejection of the unwanted band.

3. IF Amplifier

The proposed switchable harmonic mixer has a high input capacitance due to the three mixing stages. This input capacitance can limit the performance of the previous stage (sub-harmonic mixer) due to the high operating frequency. Reducing the input capacitance comes on the cost of reducing the conversion gain and increasing the noise figure. To overcome this problem, an IF amplifier, used as a buffer, is implemented between the sub-harmonic and switchable harmonic mixers. This amplifier, shown in Fig. 62, employs shunt peaking to provide higher gain at the 10.5 GHz band. The higher gain is necessary to compensate for the systematic gain difference of 9 dB between the two bands as pointed out in Table VI, and the gain reduction due to the parasitic capacitances. Another advantage of the IF amplifier is reducing the noise figure of the overall switchable harmonic mixer because it provides an additional gain.

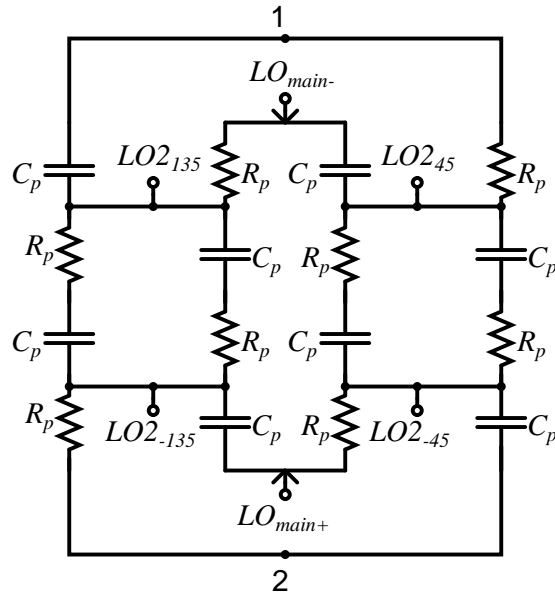


Fig. 60. Two-stage poly-phase shifter.

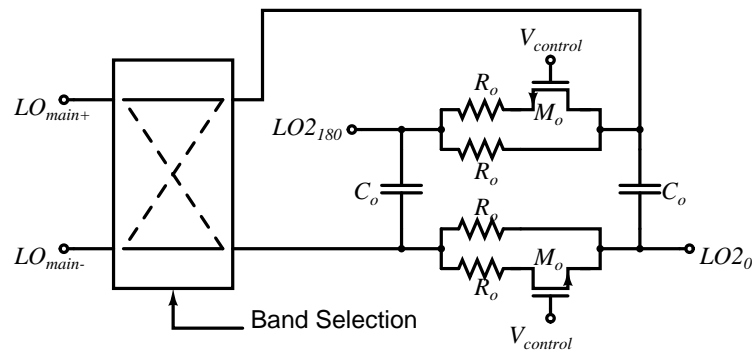


Fig. 61. RC phase shifter with electronic tuning.

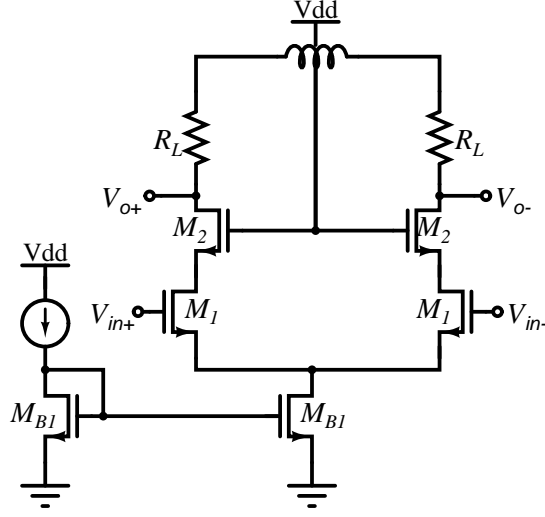


Fig. 62. IF amplifier with shunt peaking.

The cascode architecture is used to ensure stability of the amplifier.

4. IF Amplifier and Switchable Harmonic Mixer Simulation Results

The post-layout simulation results for the conversion gain of the switchable harmonic mixer and IF amplifier versus the baseband frequency for the 3.5 and 10.5 GHz frequency bands is shown in Fig. 63. The mixer has a conversion gain of 6.7 and 5.2 dB for the 3.5 and 10.5 GHz bands, respectively. Only 1.5 dB difference in gain is achieved due to the effect of the gain peaking introduced by IF amplifier. Simulations also showed a rejection higher than 60 dB. This value is hard to achieve without a tuning scheme in the measurement as mentioned in Section II.D and will be shown in Section IV.

A simulated noise figure of 17.1 and 18 dB at baseband are obtained for the 3.5 and 10.5 GHz frequency bands, respectively. The 10.5 GHz band has slightly higher noise figure due to the additional losses. The IIP3 of the mixer and IF amplifier is

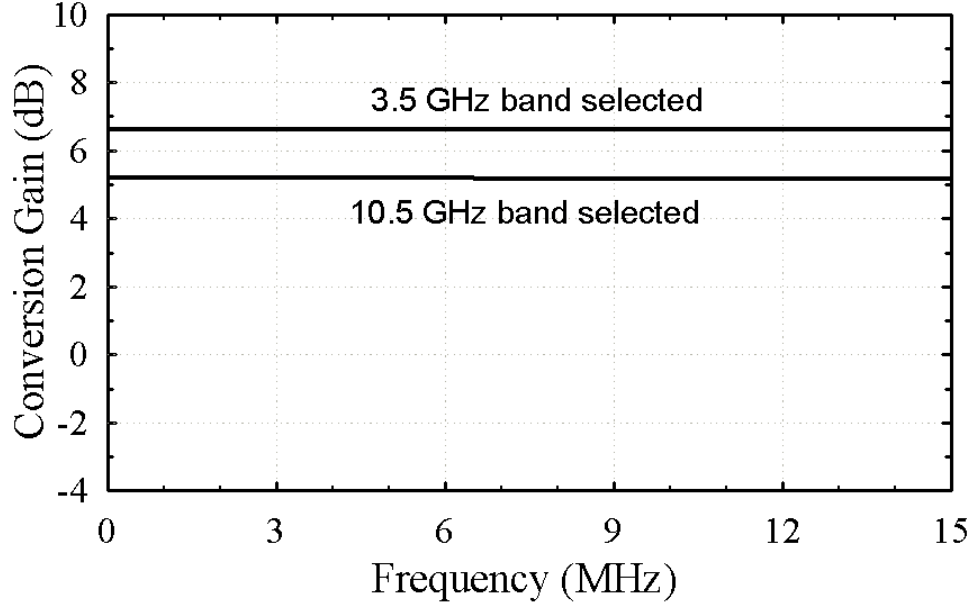


Fig. 63. Conversion gain for the 3.5 and 10.5 GHz frequency bands versus the baseband frequency.

7 and -1 dBm for 3.5 and 10.5 GHz band, respectively. Simulations are performed with a two-tone separation of 10MHz. The IIP3 at the 10.5 GHz is lower due to the effect of the higher gain introduced by the shunt peaking IF amplifier. However, the -1 dBm IIP3 is still within the required specification. The total current consumption of this mixer is 15 mA including the IF amplifier.

E. Experimental Results

The switchable harmonic receiver is fabricated using 0.18 μm BiCMOS technology provided by Jazz Semiconductor. The cut-off frequency of this technology is 70 and 50 GHz for the BJT and MOS transistors, respectively. The die micrograph is shown in Fig. 64, where the total area is 0.7 mm², excluding pads. A printed circuit board (PCB), shown in Fig. 65 is designed to test the dual-band receiver. The chip is pack-

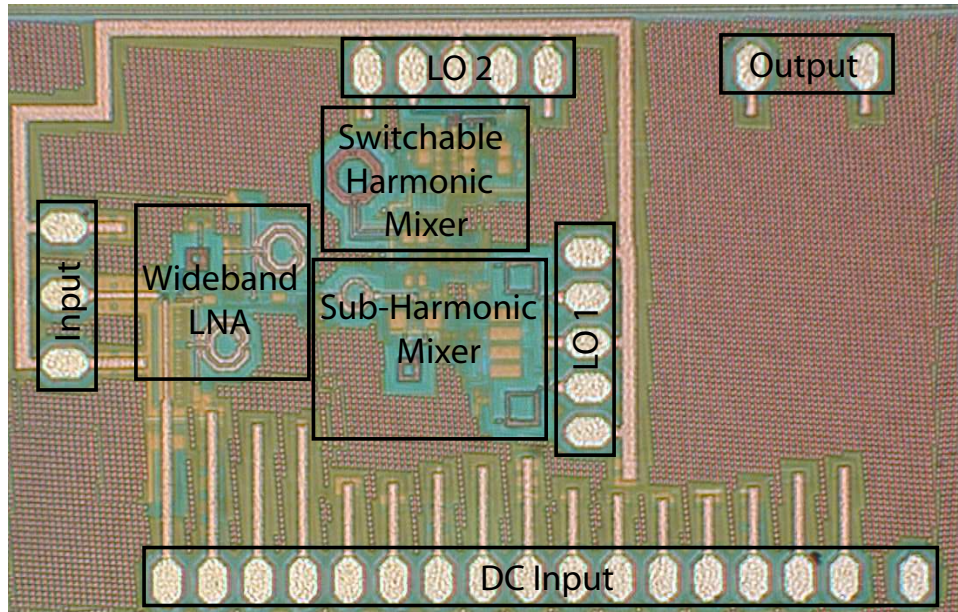


Fig. 64. Die photo of the switchable harmonic receiver.

aged in a quad flat no lead (QFN) package. The input signal is injected using a GSG RF probe, while the output of the receiver is applied to an off-chip instrumentation amplifier for the differential to single-ended conversion necessary for the measurements. The 3.5 and 10.25 GHz local oscillator signals are applied externally and injected to the chip through SMA connectors. Ground is applied from several locations on the board to provide a clean ground across the whole PCB. Agilent N5230A network analyzer is used to inject the mm-wave signal and to measure the return loss of LNA. LO signals are applied using HP-8673C signal generator and HP 8719ES network analyzer. The single-ended output is measured with HP 3588A spectrum analyzer.

The overall measured conversion gain versus the baseband frequency (DC-15 MHz) for both 24 and 31 GHz frequency bands is shown in Fig. 66. These plots are obtained by measuring the output signal using HP 3588A spectrum analyzer and

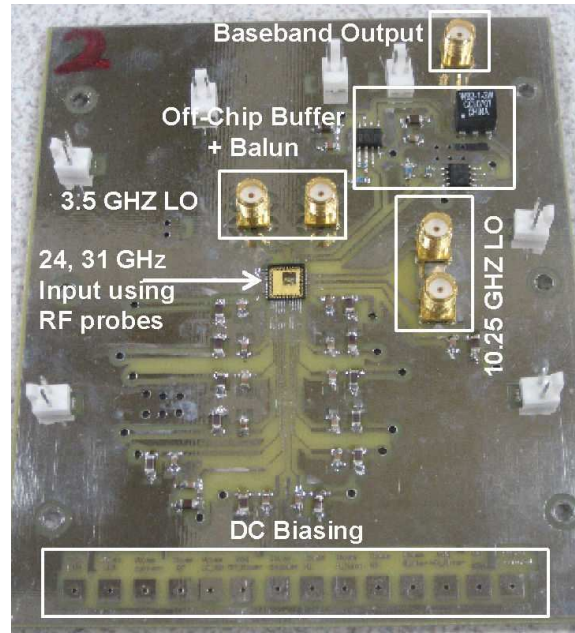


Fig. 65. Designed printed circuit board for the switchable harmonic receiver.

subtracting the gain of the off-chip amplifier. An overall conversion gain of 21 and 18 dB is measured for 24 and 31 GHz frequency bands, respectively.

Fig. 67 shows the spectrum of the output signal for various conditions. Fig. 67(a) demonstrates the case where the 24 GHz band is selected and 31 GHz band is rejected, while Fig. 67(b) presents the opposite scenario. In this measurement the 24 and 31 GHz input signals are adjusted to have the same amplitude. Measurements show a rejection of the unwanted signal better than 43 dB for two different cases after manual tuning of the phase and amplitude mismatches. The widening in the down-converted 31 GHz is due to the input Agilent N5230A network analyzer that is used to generate the 31 GHz input signal. Comparing the amount of rejection with the existing low giga-hertz dual band receiver, the implemented dual-band receiver achieves the same amount of rejection in spite of the operation at mm-wave frequen-

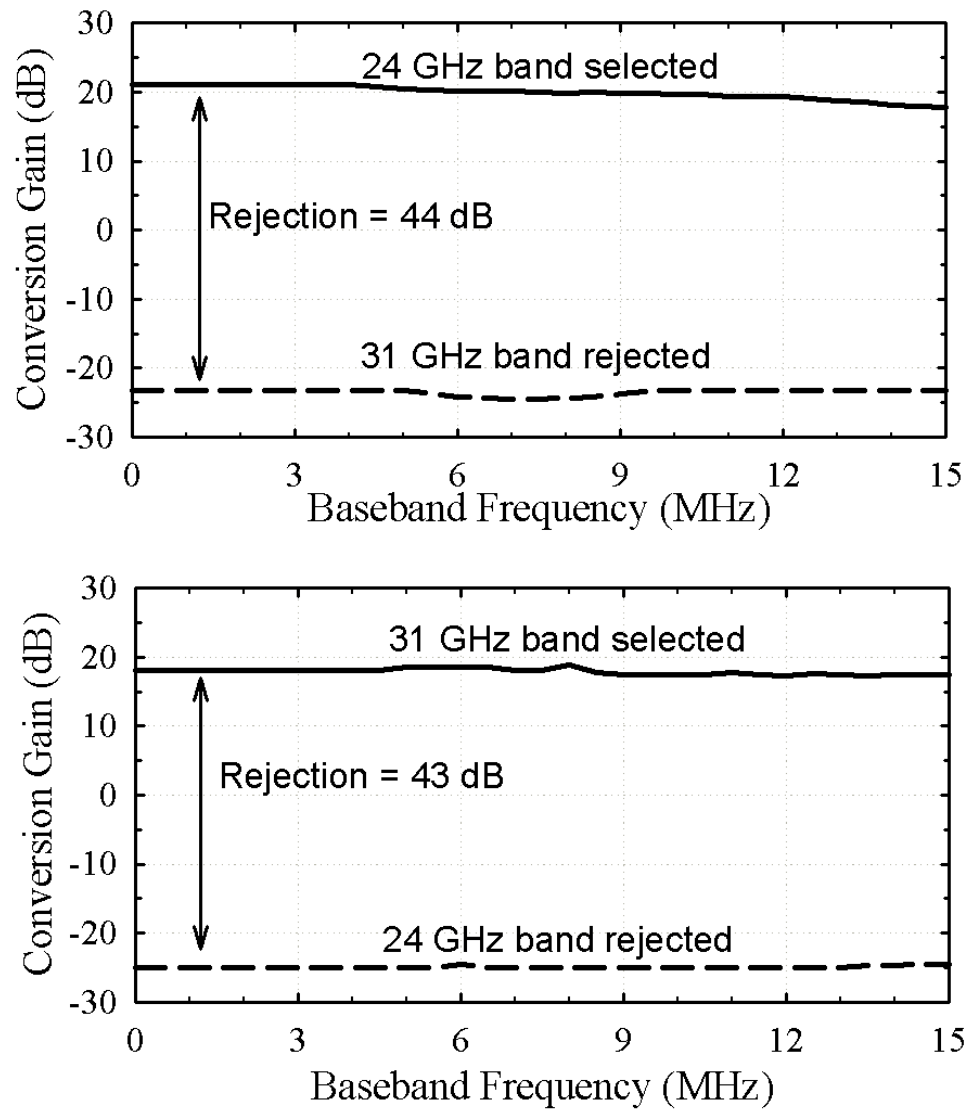
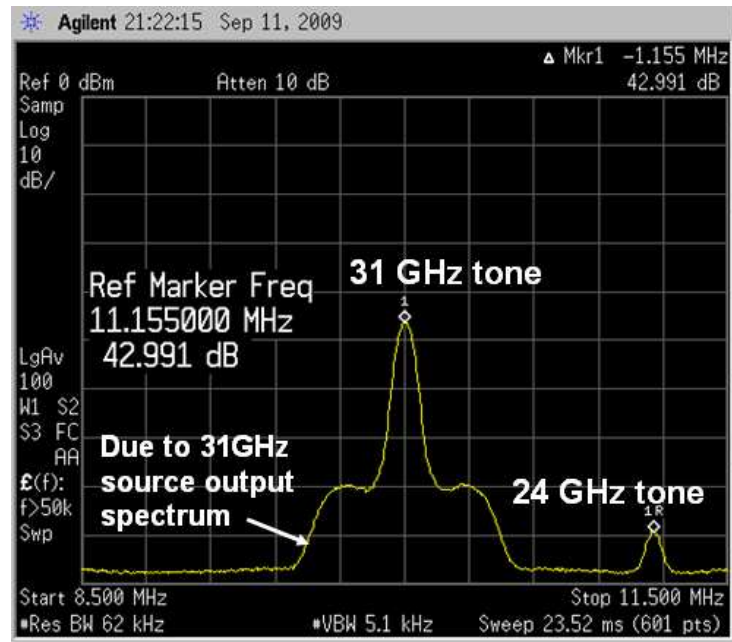


Fig. 66. Measured conversion gain and rejection of the proposed switchable harmonic receiver.

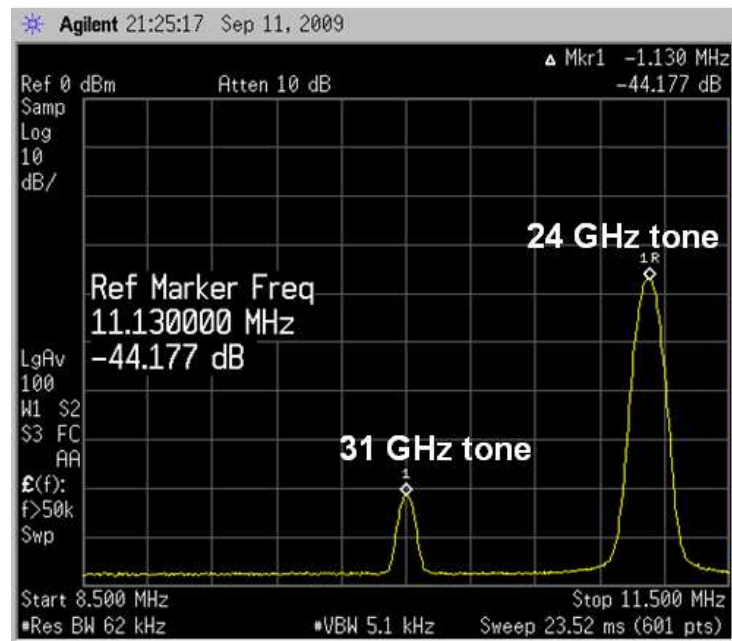
cies. The simulation results show a rejection better than 60 dB. The discrepancy is mainly due to mismatches, inaccurate models, and substrate coupling. Automatic tuning schemes can be applied later for this dual-band receiver to increase the amount of rejection.

Fig. 68 shows the measured rejection versus the phase control voltage, $V_{\phi,control}$, when the amplitude control (Fig. 59) is kept at its default value. As depicted, optimum values of phase control voltage for maximum rejection of 24 and 31 GHz bands are 0.3 and 0.24 V respectively. Optimum values are different for the two bands because the mismatches and process variations have a different impact on the rejection for the fundamental and third order harmonic components. This optimum value can be obtained using an automatic tuning scheme.

Non-linearity measurements is performed for both 24 and 31 GHz frequency bands. The DC-40 GHz Agilent N5230A network analyzer and 60 GHz signal generator are used as the input source. The two input signal tones are applied with a separation of 1.2 MHz. The main output signal tones are at 7 and 8.2 MHz and the third order intermodulation signal appears at 9.4 MHz. The measured output spectrum shows difference between main tones and the third order intermodulation tone is 44 dB for the 24 GHz. This result in an output referred third order intercept point (OIP3) of 3 dBm which is equivalent to an input referred third order intercept point (IIP3) of -18 dBm. Similar steps are performed for the 31 GHz band, and an IIP3 of -17 dBm is obtained. The measured noise figure is 8 and 9.5 dB for the 24 and 31 GHz band, respectively. The complete dual-band receiver consumes 60 mW from a 1.8 V. Finally, the complete performance summary of the switchable harmonic receiver and its building blocks is shown in Table IX.



(a)



(b)

Fig. 67. Measured rejection when (a) the 24 GHz band or (b) the 31 GHz band is selected.

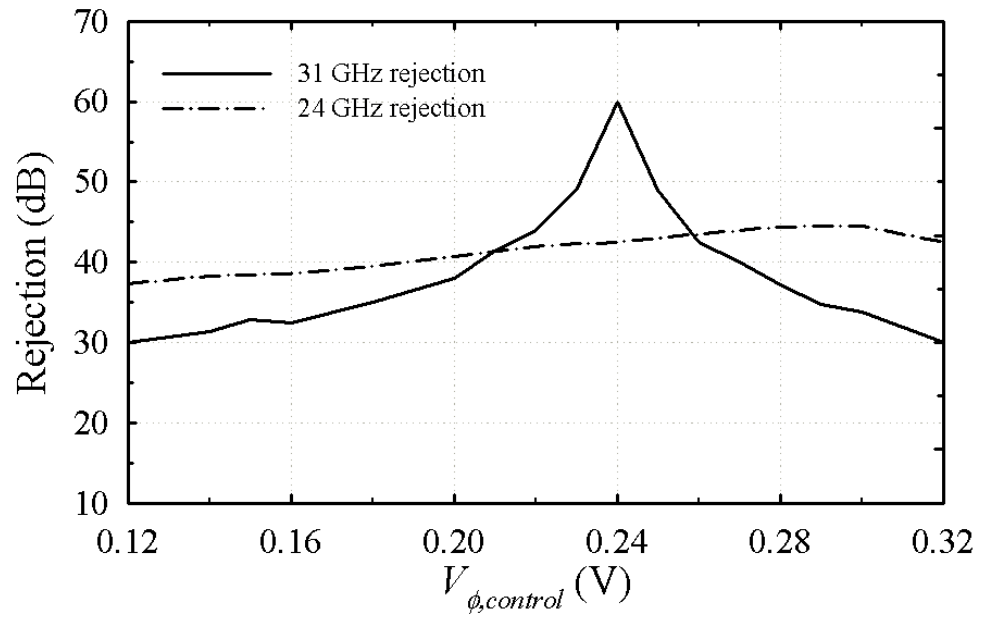


Fig. 68. Measured rejection versus phase control voltage, $V_{\phi,control}$ when 31 or 24 GHz band is rejected.

Table IX. Dual-band switchable harmonic receiver performance summary.

Parameter	Measured	Parameter	Measured
LNA		Overall Receiver Front-End	
Gain (dB)	12	Technology	0.18 μm BiCMOS
NF (dB)	<6	$f_{T,BJT}/f_{T,MOS}$ (GHz/GHz)	70/50
IIP3 (dBm)	>-6	Supply (V)	1.8
BW (GHz)	9	Conversion Gain (dB)	21@24 GHz 18@31 GHz
Current (mA)	8	S11 (dB)	<-12
MM-wave mixer		NF@12.5 MHz (dB)	8@24 GHz 9.5@31 GHz
Gain (dB)	3	IIP3 (dBm)	-18@24 GHz -17@31 GHz
NF (dB)	>13	Total Power (mW)	60
IIP3 (dBm)	>0	Rejection of 24 GHz (dB)	43@ $V_{\phi,control} = 0.25$ V
BW (GHz)	12	Rejection of 31 GHz (dB)	44@ $V_{\phi,control} = 0.25$ V
Current (mA)	10	Total Core Area (mm^2)	0.7

F. Summary

A dual-band switchable harmonic receiver architecture was introduced in this chapter. Mathematical formulation and frequency planning of the receiver was also provided in this chapter. Mismatch analysis showed that a 2% variation in the amplitude and a phase shift of 2 degrees reduces the amount of rejection of the unwanted band to -28 dB. However, automatic tuning can increase the amount of rejection. A prototype was fabricated using 0.18 μm BiCMOS technology with 0.7 mm^2 of chip area. The receiver was implemented for the ISM and LMDS bands at 24 and 31 GHz, and it was targeting the IEEE802.16 standard. Measurements showed a band rejection higher than 43 dB, gain higher than 18 dB, NF lower than 9.5 dB, and IIP3 higher than -17 dBm. The receiver consumed 60 mW from a 1.8 V supply.

CHAPTER IV

A CMOS LOW NOISE AMPLIFIER WITH RECONFIGURABLE INPUT MATCHING NETWORK

A. Introduction

One of the challenging building blocks in multi-band/multi-standard receivers is the LNA. Parallel, concurrent, or wideband LNAs are the commonly used approaches employed in multi-function receivers as demonstrated in Fig. 69 [12, 13, 68, 69]. Parallel LNAs are achieved by using several LNAs for each band/standard [12]. This approach requires additional area for various LNAs in addition to switches for band selection, which increases the complexity of the receiver. Concurrent LNAs provide dual input matching at two different frequency bands [13], and wideband LNAs provide wideband matching [68]. Concurrent and wideband LNAs occupy less area at the cost of higher requirement on the 1 dB compression point, and hence higher power consumption. The higher 1 dB compression point is because several bands have to be amplified by the LNA before the desired band is selected.

Solving the tradeoff between area and power consumption for multi-band/multi-standard LNAs is currently one of the main challenges. Designing a reconfigurable narrow-band LNA solves this challenge by passing only the desired band to the receiver. Recently, a reconfigurable LNA has been proposed to solve this dilemma [70]. In this architecture discrete tuning is utilized for band selection. However, this is not efficient for selecting a large number of bands, because it relies on adding a new inductor for each additional band, hence increasing the area of the LNA. A multi-band positive feedback LNA for the UMTS, 802.11b-g and DCS1800 standards was also reported [71]. This approach uses a common-gate topology along with a positive feed-

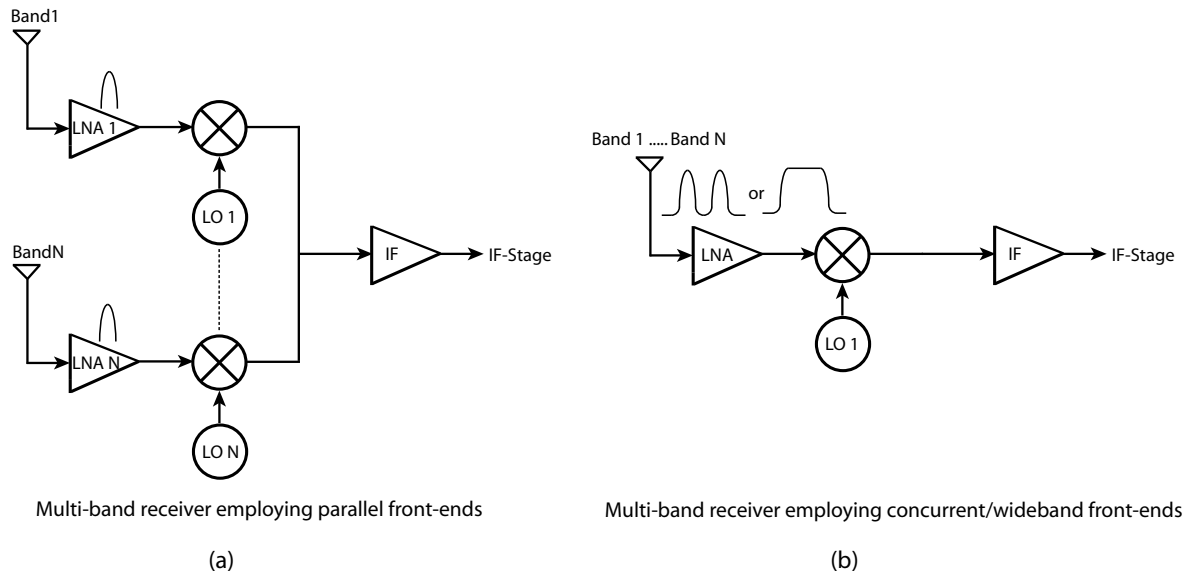


Fig. 69. Receiver architectures employing (a) parallel and (b) concurrent/wideband front-ends.

back to provide the discrete tuning of the input matching network for the three bands. In this approach, stability is an important factor that needs to be carefully considered during the design phase. The approach results in high noise figure and power consumption. Also, the linearity of this approach is limited as a result of the positive feedback which reduces the overdrive voltage across the main transistor. Another approach was reported for 750 MHz - 3 GHz frequency range [72]. The reconfigurable LNA uses a two-stage architecture where the first stage is a wideband LNA and the second stage provides band selection through an active recursive bandpass filter. The main advantage of this approach is removing any on-chip inductor. However, this approach results in high noise figure, low linearity, and high power consumption.

In this work, a new continuous reconfigurable LNA is proposed. Continuous tuning is preferred over discrete tuning as in [70, 71] because it is less sensitive to process variations. Any shift in the performance can be electronically tuned using

the proposed architecture. In addition, for larger number of frequency bands, discrete tuning is not suitable as it is harder to design for good input matching and it necessitates additional components (such as inductors), which increases the overall area of the LNA. The proposed LNA is characterized by its continuous tuning, lower noise figure compared to the active recursive bandpass filter and the positive feedback approaches in [71, 72], respectively. Similar linearity is achieved when compared to the single-band LNAs. In addition, the presented architecture does not require higher linearity similar to the wideband approach, due to its narrow-band nature. The proposed tuning technique is not only suitable for tuning the matching network, but also can be used to scale the inductance value for any application.

B. Narrow-Band Low Noise Amplifier

The common approach for designing a narrow-band LNA is to use a cascode amplifier with inductive degeneration as shown in Fig. 70 [29]. This architecture provides simultaneous input matching and low noise figure (NF). The output tank circuit is tuned to the required band, and the input series resonant circuit is adjusted to provide sufficient matching at the desired frequency band. For this LNA, the input impedance is approximately calculated from [29]

$$Z_{in} = j\omega \cdot (L_g + L_s) + \frac{1}{j\omega \cdot c_{gs1}} + \omega_T L_s, \quad (4.1)$$

where ω is the frequency of operation in radians per seconds, ω_T is the transistor cutoff frequency in radians per seconds, and c_{gs1} is the gate source capacitance of the main transistor, M_1 . The real part of the input impedance, Z_{in} , is adjusted using the source inductor L_s , while the imaginary part is removed at the resonant frequency using the inductor L_g .

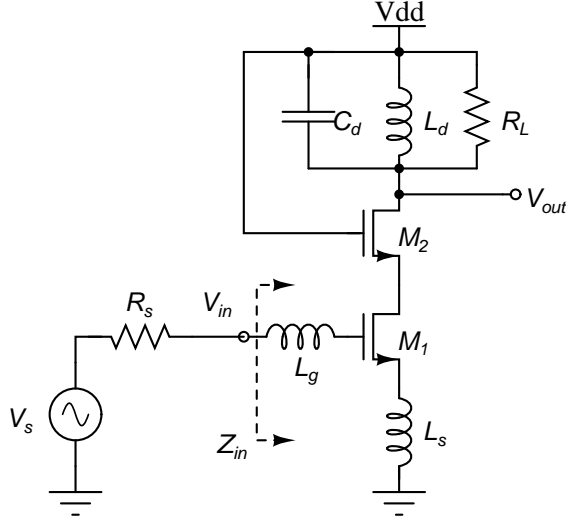


Fig. 70. Conventional narrow-band LNA architecture (biasing is not shown).

The noise figure, $NF(\omega_o)$, and the gain, $A(\omega_o)$, at the resonance frequency, ω_o , are obtained by [29]

$$NF(\omega_o) = 1 + \chi \cdot \gamma \cdot g_{do(M1)} \cdot R_s \left(\frac{\omega_o}{\omega_T} \right)^2, \quad (4.2)$$

$$A(\omega_o) = \frac{R_L}{2R_s} \cdot \frac{\omega_T}{\omega_o}, \quad (4.3)$$

$$\omega_o = \frac{1}{\sqrt{(L_g + L_s) \cdot c_{gs1}}}, \quad (4.4)$$

where $g_{do(M1)}$ is the zero bias drain transconductance of M_1 , γ is the noise coefficient, χ is the excess noise factor due to the gate noise, R_s is the source resistance, and R_L is the load resistance.

The NF defined in (4.2) is the lowest noise figure that can be obtained from this architecture while the input is perfectly matched and the output is tuned to the operating frequency [29]. The same conclusion holds for the gain defined in (4.3). These results indicate that the performance of the narrow-band LNA depends on the

resonant frequency, which is adjusted using the inductor L_g at the input matching network, and inductor L_d and capacitor C_d at the output tank circuit.

To achieve an LNA with optimum performance (gain, noise figure and linearity) across a wide frequency range, the inductor L_g or the capacitor c_{gs1} has to be changed for each operating frequency. Tuning the value of c_{gs1} changes the cut-off frequency and hence the inductor L_s should also be tuned to achieve the perfect matching. On the other hand, tuning L_g does not require any additional component to be tuned. Tuning L_g is a challenging problem because the additional circuitry should not increase the noise figure, degrade the linearity or affect the gain of the LNA. In addition, it is not trivial to tune a floating inductor. One simple approach is to place several inductors in parallel, and switch among them. In this case, the active switch loss and its non-linear behavior degrade the noise figure and linearity of the LNA considerably. On the other hand, switching among various inductors does not provide a continuous tuning scheme. In this work, a new tuning scheme for the inductor L_g is proposed. This tuning scheme is applied to the narrow-band LNA to achieve a reconfigurable input matching network.

The load of the LNA can be either a tunable tank circuit with a bank of capacitors or a wideband load over the tuning range. In this work, two resonant circuits are used to provide a constant load across the frequency range for simplicity.

C. Proposed Tunable Floating Inductor

1. Basic Idea

Fig. 71(a) shows a model for the conventional input matching network of the LNA. In this model, the input impedance of the LNA is combined into a single term, Z_{LNA} ,

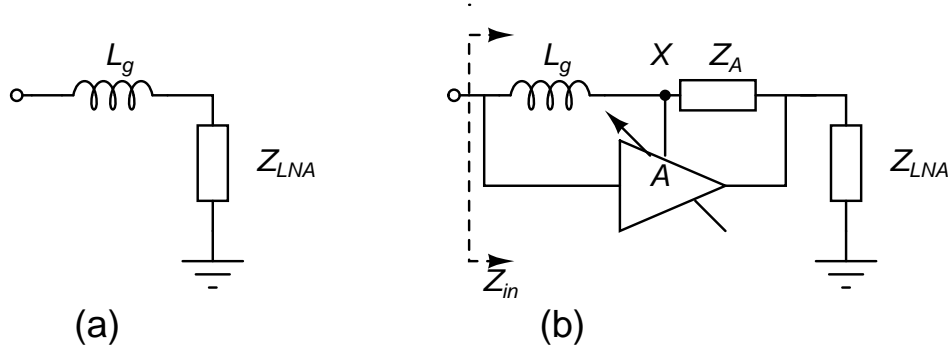


Fig. 71. (a) Input Matching Network of the conventional LNA (b) Proposed tunable floating inductor basic architecture.

where

$$Z_{LNA} = j\omega \cdot L_s + \frac{1}{j\omega \cdot c_{gs1}} + \omega_T L_s. \quad (4.5)$$

As discussed earlier in section B, the input matching network is tuned by changing the value of the inductor L_g . To achieve this goal, the input matching network is modified according to Fig. 71(b) where an ideal amplifier is placed to provide the necessary scaling for L_g . The input impedance of this architecture is calculated from

$$Z_{in} = j\omega \cdot L_g(1 - A(Z_A)) + Z_{LNA}, \quad (4.6)$$

where $A(Z_A)$ is the voltage gain of the amplifier, and Z_A is an impedance used to change the gain of the amplifier, as discussed later in this section. Based on eq. (4.6), the inductor L_g is scaled by the amplifier with the factor $(1 - A(Z_A))$. Depending on the polarity of the gain, the inductor value can either increase or decrease. In this architecture, the common node of the amplifier (node X in Fig. 71(b)) is floating and not connected to the ground of the circuit.

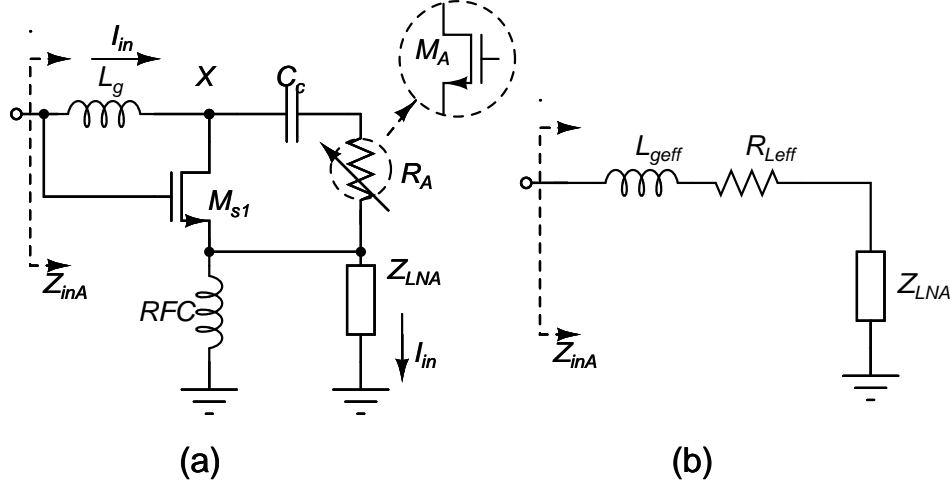


Fig. 72. (a) Proposed tunable floating inductor architectures based on a common drain configuration (C_c is decoupling capacitor). (b) Equivalent RL model of the common drain tunable architecture.

2. Practical Implementations

Several approaches can be used to implement the proposed amplifier. A common drain configuration is considered, and the associated non-idealities and their effect in the inductance tuning is presented. Common source configuration is another implementation that increases the effective inductance value. However, this implementation leads to higher noise figure. Common gate architecture is not considered because it has a small input impedance, which affects the overall input impedance of the architecture shown in Fig. 71(b), and therefore the tuning of the inductor.

Common Drain Configuration: The common drain configuration is shown in Fig. 72(a), where the common node is connected to the node X. The impedance Z_A is replaced by a variable resistance R_A to provide the necessary inductance tuning. This resistance is implemented using a transistor biased in the triode region, M_A . Transistor M_{s1} is the main transistor of the common drain amplifier. The biasing of

this stage is done through an RF choke coil to lower the noise figure of the LNA. The input impedance of this architecture is calculated from

$$Z_{inA} = \frac{j\omega \cdot L_g}{1 + g_{m(Ms1)} \cdot R_A} + \frac{R_A}{1 + g_{m(Ms1)} \cdot R_A} + Z_{LNA}, \quad (4.7)$$

where $g_{m(Ms1)}$ is the transconductance of the main transistor. Note that $A(R_A)$ in (4.6) is $\frac{g_{m(Ms1)} \cdot R_A}{1 + g_{m(Ms1)} \cdot R_A}$ for a common drain configuration. As can be noticed, the ideal model in (4.6) does not predict the additional resistive term in (4.7). This additional resistive term in (4.7) is due to the finite output impedance of the amplifier, which was not considered in the basic idea for simplicity. The proposed tunable architecture can be modeled by a series RL equivalent circuit as shown in Fig. 72(b), with

$$L_{geff} = \frac{L_g}{1 + x_T}, \quad (4.8)$$

$$R_{Leff} = \frac{R_A}{1 + x_T}, \quad (4.9)$$

where L_{geff} is the effective inductance and R_{Leff} is the non-ideal resistance that appear due to this architecture. x_T is the tuning coefficient defined as

$$x_T = g_{m(Ms1)} \cdot R_A. \quad (4.10)$$

Eq. (4.8) shows that this architecture reduces the effective inductance value by either increasing the transconductance or the resistance R_A . Fig. 73 shows L_{geff} versus the tuning coefficient (x_T). This simulation is performed using Spectre¹ for $f_o = 1$ GHz and $L_g = 10$ nH, where the transistor M_{s1} is replaced with an ideal voltage controlled current source. For the common drain configuration, real inductor L_g is larger than L_{geff} , however, having a larger inductor is better if compared to having several inductors in parallel for band selection. The non-ideal resistive term, R_{Leff} ,

¹Spectre 5.1, Cadence, 2007

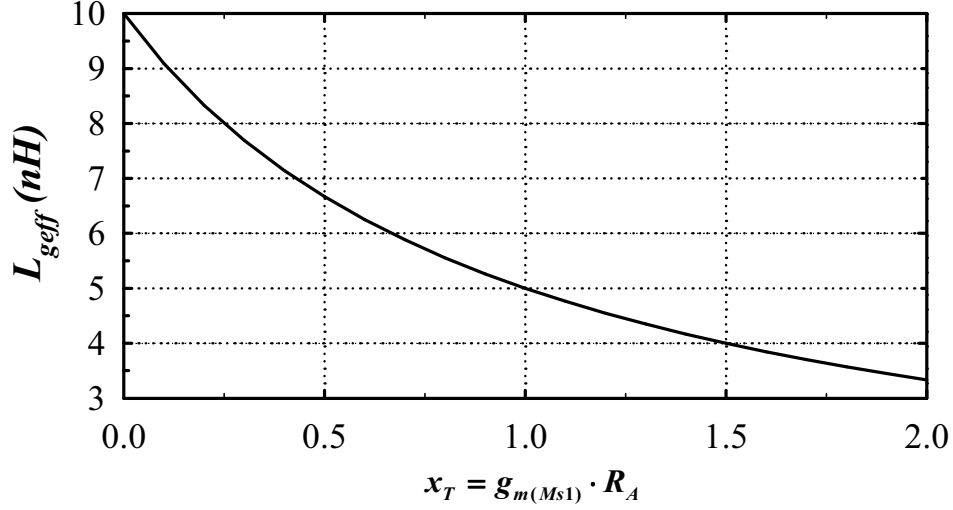


Fig. 73. Effective inductance value versus the tuning coefficient, x_T , ($L_g = 10$ nH and $f = 1$ GHz) for the architecture shown in Fig. 72(a).

introduces additional loss, which lowers the quality factor of the tunable inductor. In this case, the effective quality factor, Q_{LA} , for the ideal inductor L_g ($r_{Lg} = 0$) is found as

$$Q_{LA} = \frac{\omega \cdot L_g}{R_A}. \quad (4.11)$$

The quality factor in this architecture does not depend on the transconductance of M_{s1} , and it depends only on the resistance R_A . It should be mentioned that the parasitic capacitance changes the inductive behavior of the proposed tunable inductor architecture at higher frequencies. Therefore during circuit simulations, it is important to take into account this non-ideal effect. In this implementation, the additional circuit consumes 40% of the total power. The noise contribution of the additional tuning circuit mainly depends on the additional power consumption. The

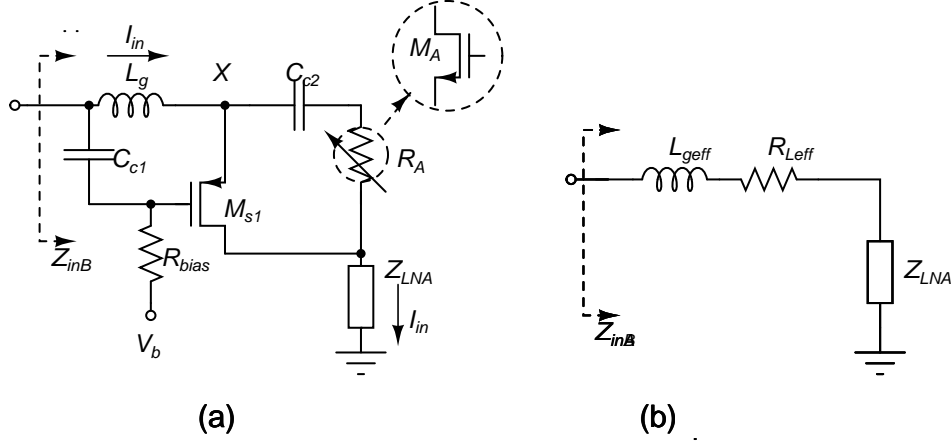


Fig. 74. (a) Proposed tunable floating inductor architectures based on a common source configuration (C_{c1} , C_{c2} and R_{bias} are decoupling capacitances and bias resistance, respectively). (b) Equivalent RL model of the common source tunable architecture.

noise contribution of the tuning circuit and its dependency to the tuning range will be discuss later.

Common Source Configuration The second architecture is shown in Fig. 74(a), where a common source amplifier is used instead of the common drain one. Similar to the first implementation in Fig. 72(a), the impedance Z_A is replaced with the variable resistance R_A for tuning the inductance value. In this case, the input impedance, Z_{inB} , and the quality factor, Q_{LB} , are calculated from

$$Z_{inB} = j\omega \cdot L_g \cdot (1 + g_{m(Ms1)} \cdot R_A) + R_A + Z_{LNA}, \quad (4.12)$$

$$Q_{LB} = \frac{\omega \cdot L_g \cdot (1 + g_{m(Ms1)} \cdot R_A)}{R_A} \approx \omega \cdot L_g \cdot g_{m(Ms1)}. \quad (4.13)$$

The effective inductance value increases by increasing the product $g_{m(Ms1)} \cdot R_A$ as shown in (4.12). In addition, the quality factor highly depends on the transduc-

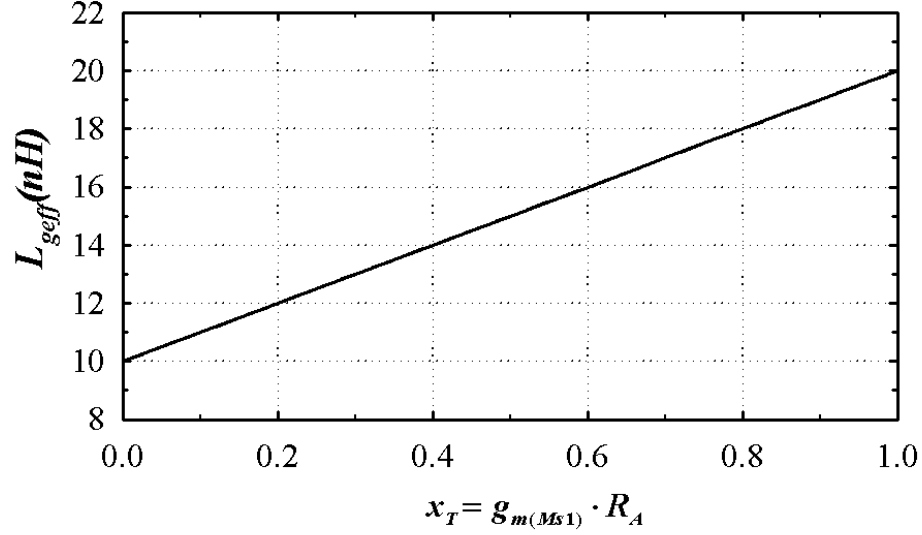


Fig. 75. Effective inductance value versus the product $g_{m(Ms1)} \cdot R_A$ ($L_g = 10$ nH and $f_o = 1$ GHz) for the architecture in Fig. 74(a).

tance of the main transistor. For higher gains, the quality factor does not depend on the resistance R_A . The simulated effective inductance versus the product $(g_{m(Ms1)} \cdot R_A)$ is shown in Fig. 75, using a voltage controlled current source for the transistor M_{s1} in Spectre while $L_g = 10$ nH and $f = 1$ GHz. Also, higher quality factor is obtained for higher $(g_{m(Ms1)} \cdot R_A)$ values, and it is proportional to the increase in the inductance value.

Depending on the application, either one of these proposed configurations can be used. The main design factors that determine which configuration to use are the tuning range, the quality factor, the linearity, and the additional noise due to the proposed circuitry. Common drain configuration is characterized by its lower noise contribution because most of the noise is circulating in the loop consisting of M_{s1} and R_A . For the common source configuration, most of the noise flows through Z_{LNA} , and hence increases the overall noise figure of LNA. In addition, common source

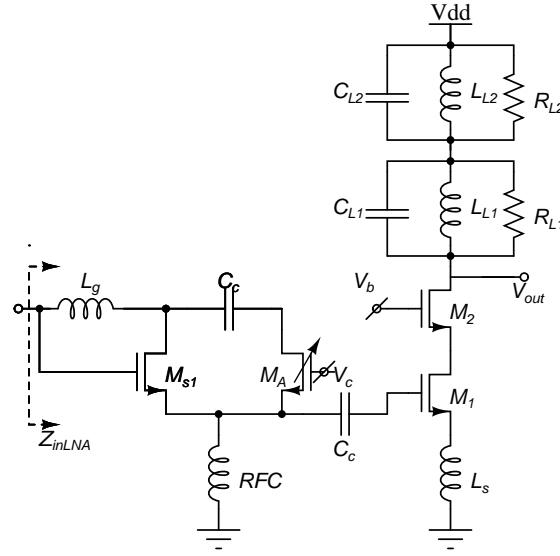


Fig. 76. The proposed reconfigurable low noise amplifier (biasing circuit not shown).

configuration requires additional capacitor (C_{cl}) and resistance (R_{bias}) to bias M_{s1} , as shown in Fig. 74.

Based on the above discussion, the common drain configuration is selected to provide the required tuning of the inductor L_g . In the next section, the complete architecture of the proposed LNA and the mathematical analysis of performance parameters is demonstrated.

D. Reconfigurable Low Noise Amplifier

The complete architecture of the proposed reconfigurable low noise amplifier is shown in Fig. 76. In this architecture, the reconfigurable input matching network is realized using the tunable inductor common drain configuration discussed in section 2. The output load is realized using two resonant circuits, each tuned at a different frequency. This approach increases the bandwidth of the load to cover the frequency range,

however the effective load resistance (gain) is reduced. Placing the two resonant circuits farther apart results in a non-constant load with respect to frequency. Hence, this approach is not suitable for covering a large bandwidth. For a larger bandwidth, it is preferred to use a bank of capacitors and a varactor for narrow-band output tuning.

1. Input Impedance

The input impedance of the LNA in Fig. 76 is

$$\begin{aligned} Z_{inLNA} &= \frac{j\omega \cdot L_g}{1 + x_T} + \frac{R_A}{1 + x_T} \\ &+ j\omega \cdot L_s + \frac{1}{j\omega \cdot c_{gs(M1)}} + \omega_T \cdot L_s. \end{aligned} \quad (4.14)$$

For this case, the resonant frequency, f_o , and the input impedance, Z_{inLNA} , at resonance are determined from the following equations

$$\begin{aligned} f_o &= \frac{1}{\sqrt{c_{gsM1} \cdot (L_s + \frac{L_g}{1+x_T})}} \\ &\approx \frac{\sqrt{1+x_T}}{\sqrt{c_{gsM1} \cdot L_g}} \quad (L_s \ll \frac{L_g}{1+x_T}), \end{aligned} \quad (4.15)$$

$$\begin{aligned} Z_{inLNA}(f_o) &= R_{effA} + \omega_T \cdot L_s, \\ R_{effA} &= \frac{R_A}{1 + x_T}, \end{aligned} \quad (4.16)$$

Eq. (4.15) shows that for frequency tuning, either the resistance R_A or the transconductance $g_{m(Ms1)}$ can be changed. The additional resistive term, R_{effA} , which appears due to the tuning circuit can be considered as part of the real input impedance to adjust the matching, i.e. $\omega_T \cdot L_s$ can be designed for a value less than 50Ω . R_{effA} does not affect the gain of the amplifier as shown later. It is important to mention that the real part of Z_{inLNA} changes with the resonant frequency due to changing

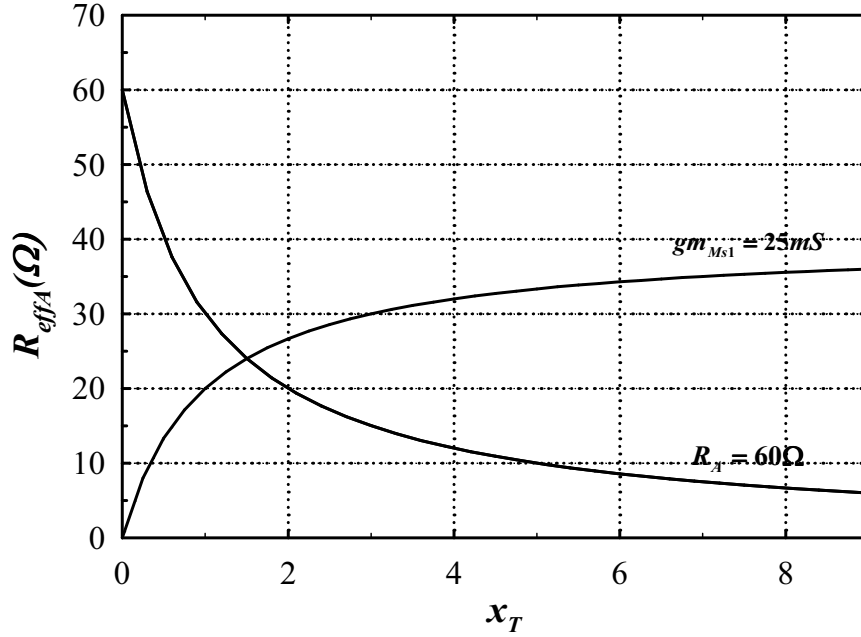


Fig. 77. R_{effA} versus the tuning factor x_T for either changing R_A or $g_{m(Ms1)}$ ($x_T = g_{m(Ms1)} \cdot R_A$).

x_T , and therefore perfect matching cannot be obtained along the whole frequency range. Fig. 77 shows the change of the effective resistance, R_{effA} versus the tuning factor (x_T), based on (4.16), if either the resistance R_A or the transconductance is changed. As can be noticed, the effective resistance increases in case of increasing the resistance R_A and keeping the transconductance constant, while it decreases when the transconductance is increased. The first case does not change the power consumption since $g_{m(Ms1)}$ is constant, while the latter changes the power consumption when the tuning frequency is changed. Hence, for good matching along a wide tuning range, it is better to change the resistance value (R_A) and keep the transconductance as high as possible to keep R_{effA} nearly constant over the tuning range.

2. Gain

The gain of the LNA, A_v , at resonance is found to be

$$A_v(f_o) = \frac{R_{Ltot}}{R_s + R_{effA} + \omega_T \cdot L_s} \cdot \frac{\omega_T}{\omega_o}. \quad (4.17)$$

Under the perfect matching condition ($R_s = R_{effA} + \omega_T \cdot L_s = 50\Omega$), the overall gain of the LNA reduces to:

$$A_v(f_o) = \frac{R_{Ltot}}{2 \cdot R_s} \cdot \frac{\omega_T}{\omega_o}. \quad (4.18)$$

where R_{Ltot} is the total load resistance at the drain of the transistor M_2 . The above equation is similar to the gain of the narrow-band LNA with inductive degeneration as shown in (4.3), and therefore, this technique does not affect the overall gain of the LNA.

3. Noise Figure

Fig. 78 shows the main noise sources that contribute to the noise figure of the low noise amplifier. The main noise sources are due to the main transistor M_1 , the resistance R_A , and the transistor M_{s1} . The noise current due to the transistor M_{s1} and the resistance R_A circulates in the loop consisting of M_{s1} and R_A . A small fraction of this noise is injected inside the main circuit of LNA, and therefore, the additional circuit does not increase the noise figure significantly. The contribution of each noise component is calculated below.

The equivalent input referred noise spectral density, $\overline{v_{ni,RA}^2}/\Delta f$, due to the re-

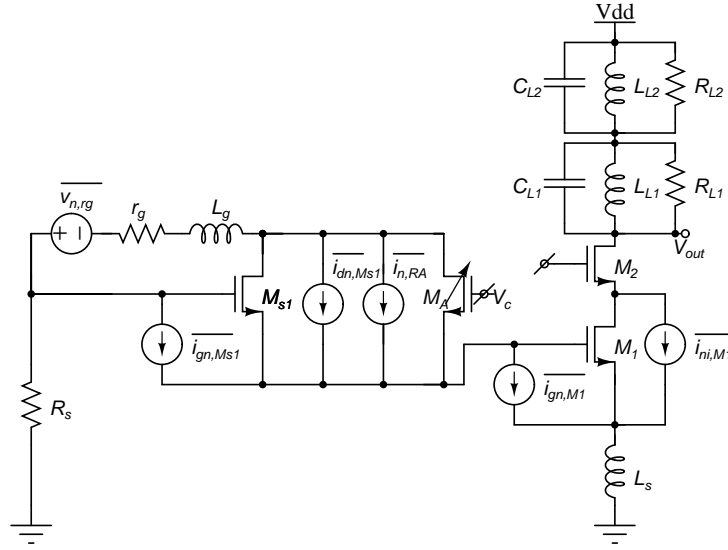


Fig. 78. Main noise sources for the proposed reconfigurable LNA.

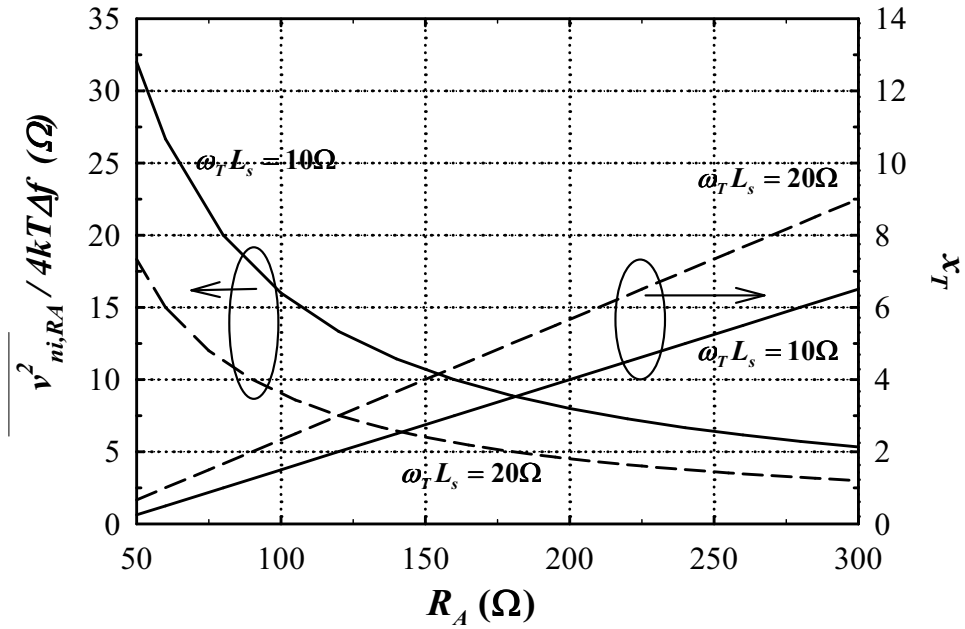


Fig. 79. Left axis : Input referred noise density of R_A , Right axis : Required tuning coefficient x_T versus the value of R_A for two cases, where $Z_{inLNA}(f_o) = 50\Omega$ ($\omega_T \cdot L_s = 10\Omega$ and $\omega_T \cdot L_s = 20\Omega$).

sistance R_A under perfect matching condition ($Z_{inLNA}(f_o) = 50\Omega$) is calculated from

$$\begin{aligned}\frac{\overline{v_{ni,RA}^2}}{\Delta f} &= 4kT \frac{R_A}{(1 + g_{m(Ms1)} \cdot R_A)^2} \\ &= 4kT \frac{x_T}{(1 + x_T)^2} \cdot \frac{1}{g_{m(Ms1)}},\end{aligned}\quad (4.19)$$

where k is Boltzmann constant and T is the temperature in kelvin. The noise of the resistance R_A can be reduced by increasing the factor $(1 + x_T)$ or increasing R_A . Fig. 79 shows the equivalent input referred noise spectral density of R_A versus its value for two cases ($\omega_T L_s = 10\Omega$, $R_{effA} = 40\Omega$ and $\omega_T L_s = 20\Omega$, $R_{effA} = 30\Omega$). Increasing the value of R_A reduces the equivalent input referred noise on the cost of increasing the transconductance $g_{m(Ms1)}$, and hence, the power consumption of the tunable inductor stage. Therefore, there is a tradeoff between noise figure and power consumption for the proposed architecture. The values of $g_{m(Ms1)}$ and x_T are determined from (4.16).

The second noise source in this architecture is the noise contributed by the transistor M_{s1} . The equivalent input referred noise spectral density due to the gate noise, $\overline{v_{ni,Mslig}^2}/\Delta f$, and drain thermal noise, $\overline{v_{ni,Mslid}^2}/\Delta f$, under perfect matching condition ($Z_{inLNA}(f_o) = 50\Omega$), are

$$\begin{aligned}\frac{\overline{v_{ni,Mslig}^2}}{\Delta f} &\approx 4kT\delta \cdot g_g \cdot \left(\frac{R_A}{1 + g_{m(Ms1)} \cdot R_A}\right)^2 \\ &= 4kT\delta \cdot \frac{\omega^2}{5\omega_T^2} \cdot \left(\frac{x_T}{1 + x_T}\right)^2 \cdot \frac{\alpha}{g_{m(Ms1)}}, \\ \frac{\overline{v_{ni,Mslid}^2}}{\Delta f} &= 4kT\gamma \cdot \left(\frac{g_{m(Ms1)} \cdot R_A}{1 + g_{m(Ms1)} \cdot R_A}\right)^2 \cdot \frac{1}{\alpha \cdot g_{m(Ms1)}} \\ &= 4kT\gamma \cdot \left(\frac{x_T}{1 + x_T}\right)^2 \cdot \frac{1}{\alpha \cdot g_{m(Ms1)}},\end{aligned}\quad (4.20)$$

where g_g is the shunt gate conductance, δ is the gate noise coefficient, and $\alpha = g_m/g_{do}$ [29]. Both the above noise sources can be combined in a single expression that

considers the correlation between the gate and drain noise.

The mathematical analysis shows that the total equivalent input referred noise density due to M_{s1} , $\overline{v_{ni,M_{s1}}^2}/\Delta f$, is

$$\begin{aligned} \frac{\overline{v_{ni,M_{s1}}^2}}{\Delta f} &= 4kT\kappa\gamma \cdot \left(\frac{x_T}{1+x_T}\right)^2 \cdot \frac{1}{g_{m(M_{s1})}}, \\ \kappa &= \frac{1}{\alpha} + \frac{\alpha\delta}{\gamma} \cdot \frac{\omega_o^2}{5\omega_T^2} + \sqrt{4\frac{\delta}{\gamma} \frac{\omega_o^2}{5\omega_T^2} \cdot c^2}, \end{aligned} \quad (4.21)$$

where c is the correlation coefficient of the gate and drain noises [29].

Fig. 80 shows the change of the input referred noise density of M_{s1} versus $g_{m(M_{s1})}$ for two cases ($\omega_T L_s = 10\Omega$, $R_{effA} = 40\Omega$ and $\omega_T L_s = 20\Omega$, $R_{effA} = 30\Omega$). As indicated in this plot, increasing $g_{m(M_{s1})}$ increases the input referred noise because higher value of R_A is required to achieve the 50Ω required matching. In addition, the tuning coefficient increases with the increase of $g_{m(M_{s1})}$.

The above analysis shows that the input referred noise depends on both $g_{m(M_{s1})}$, R_A , and $\omega_T \cdot L_s$. The analysis also shows increasing x_T lowers the noise contributions of R_A , and increases the noise contribution of M_{s1} as depicted in Figs. 79 and 80, respectively. Hence, there is an optimum solution for the design parameters (x_T , R_A , and $g_{m(M_{s1})}$) that minimizes the additional noise due to the tuning circuit for a given power consumption. This issue is addressed in more details in Section 4. The total noise spectral density due to the additional tuning circuitry, $\overline{v_{ni,c}^2}/\Delta f$, is found by adding the two input referred noise voltages in (4.19) and (4.21) resulting in

$$\frac{\overline{v_{ni,c}^2}}{\Delta f} = 4kT \cdot \left(\frac{x_T}{(1+x_T)^2} + \kappa\gamma \cdot \left(\frac{x_T}{1+x_T}\right)^2 \right) \cdot \frac{1}{g_{m(M_{s1})}}. \quad (4.22)$$

Assuming that the input referred noise spectral density of the additional circuitry is less than a specified value, $\overline{v_{ni,co}^2}/\Delta f$, (4.22) is rearranged to find the value of the

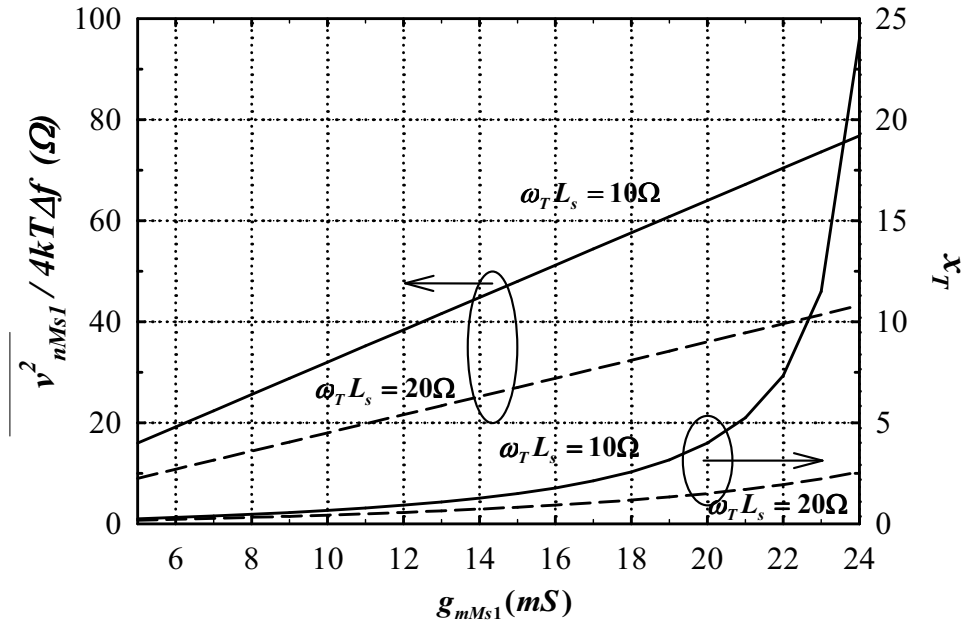


Fig. 80. Left axis: Input referred noise density of M_{s1} . Right axis: Required tuning coefficient x_T versus the value of $g_{m(Ms1)}$ for two cases, where $Z_{inLNA}(f_o) = 50\Omega$ ($\omega_T \cdot L_s = 10\Omega$ and $\omega_T \cdot L_s = 20\Omega$).

required transconductance, $g_{m(Ms1)}$

$$g_{m(Ms1)min} = \frac{4kT}{v_{ni,co}^2/\Delta f} \cdot \left(\frac{x_T}{(1+x_T)^2} + \kappa\gamma \cdot \left(\frac{x_T}{1+x_T} \right)^2 \right). \quad (4.23)$$

The above equation shows that there is a minimum value for the transconductance to satisfy the noise constraints if the tuning coefficient, x_T , is specified. This minimum value leads to minimum power consumption of the additional circuitry. The value of the resistance, R_A , is then calculated from x_T . The optimum value for the tuning coefficient is determined from the tuning range, as discussed later in Section 4.

The final major noise source, which contributes to the total noise figure, is the noise of the main transistor M_1 . For this case, the amount of noise that appears at the output is the same as the conventional low noise amplifier with inductive degeneration. Therefore, the input referred noise spectral density under perfect matching condition is [29]

$$\frac{\overline{v_{ni,M1}^2}}{\Delta f} = 4kT\chi\gamma \cdot R_s^2 \cdot \left(\frac{\omega_o}{\omega_T} \right)^2. \quad (4.24)$$

Combining equations (4.19), (4.20), and (4.24), the total noise figure of the LNA is

$$\begin{aligned} NF_T &= 1 + \gamma\chi \cdot g_{m(M1)} \cdot R_s \left(\frac{\omega_o}{\omega_T} \right)^2 \\ &+ \frac{1}{g_{m(Ms1)} \cdot R_s} \cdot \frac{x_T}{(1+x_T)^2} \\ &+ \frac{\kappa\gamma}{g_{m(Ms1)} \cdot R_s} \cdot \left(\frac{x_T}{1+x_T} \right)^2 \\ &+ \frac{r_{Lg}}{R_s} \cdot \frac{1}{(1+x_T)^2}. \end{aligned} \quad (4.25)$$

The last term in the above equation is the noise introduced by the series physical resistance of the inductor, L_g , due to its finite quality factor. As depicted, the additional noise is reduced when x_T is increased. For off-chip inductors, this term is

smaller than the other noise sources.

4. Tuning Range and Input Mismatch

The frequency of operation depends on the value of $g_{m(Ms1)}$ and R_A . Changing either of these two values changes the input resonant frequency. However, this change varies the real input impedance, as described in (4.16). Smaller variations in the real input impedance require larger tuning coefficients, which results in higher transconductance, and hence higher power consumption (Fig. 77). In the actual design, the tuning coefficient is not much higher than one, leading to a mismatch at the input of the LNA. Therefore there is a tradeoff between the mismatch and the power consumption of the additional circuitry along the tuning range. To find the optimum design parameters of the proposed architecture for a defined mismatch, a numerical approach has been developed. This numerical approach relies on solving a set of equations to find the minimum power consumption for a given mismatch and tuning range. The mismatch, Δ_m , along with the tuning range is estimated from the following equation

$$\begin{aligned}\Delta_m &\geq \frac{R_{Ah}}{1 + x_{Th}} - \frac{R_{Al}}{1 + x_{Tl}} \\ &= \left(\frac{x_{Th}}{1 + x_{Th}} - \frac{x_{Tl}}{1 + x_{Tl}} \right) \cdot \frac{1}{g_{m(Ms1)}},\end{aligned}\quad (4.26)$$

where the subscripts h and l are for the higher and lower frequency bands, respectively.

The tuning range, n_f , for the proposed LNA is derived from (4.15), and is:

$$n_f = \frac{f_h}{f_l} = \sqrt{\frac{1 + x_{Th}}{1 + x_{Tl}}}. \quad (4.27)$$

Equations (4.26) and (4.27) are two equations with three unknowns (x_{Tl} , x_{Th} , and $g_{m(Ms1)}$) and therefore they cannot be solved to find the optimum solution. The third equation is the one defined in (4.23), where the high tuning coefficient is written

in terms of the transconductance as follows:

$$\begin{aligned} x_{Th} &= \frac{2 \cdot \eta - 1 + \sqrt{(2 \cdot \eta - 1)^2 + 4 \cdot \eta \cdot (\kappa\gamma - \eta)}}{2 \cdot (\kappa\gamma - \eta)}, \\ \eta &= \frac{g_{m(Ms1)} \cdot \overline{v_{ni,co}^2} / \Delta f}{4kT}. \end{aligned} \quad (4.28)$$

In the above equation, x_{Th} is only considered because it results in a higher input referred noise, while for x_{Tl} lower input referred noise is obtained. The set of the equations in (4.26), (4.27), and (4.28) are solved numerically to find the values of $g_{m(Ms1)}$, x_{Tl} , and x_{Th} , and hence, R_{Al} and R_{Ah} . For our design, the targeted tuning range is 1.9-2.4 GHz and the overall noise figure is 3 dB. Fig. 81 shows the numerically calculated $g_{m(Ms1)}$ versus the percentage noise contribution of the additional circuitry to the total input referred noise, $\overline{v_{ni,total}^2}$, for different mismatch values ($\kappa\gamma = 2$). As depicted from Fig. 81, the required transconductance increases for lower noise contribution. This presents the tradeoff between the noise figure and the power consumption of the proposed tuning circuit. The gray area represent the region where x_{Tl} is negative. This value is not realizable with the common drain configuration. For this design, a 35% noise contribution and a mismatch, Δ_m , of 6 Ω are assumed. This results in an increase of 40% of the total power consumption of the reconfigurable LNA due to the additional circuit when compared to a single-band LNA. For this case, the calculated $g_{m(Ms1)}$ is 46 mS, x_{Th} is 1.2, and x_{Tl} is 0.38, which result in R_{Ah} and R_{Al} of 24.5 Ω and 7.2 Ω , respectively.

It is important to mention that this technique is valid for a wide tuning range by properly selecting the tuning coefficient.

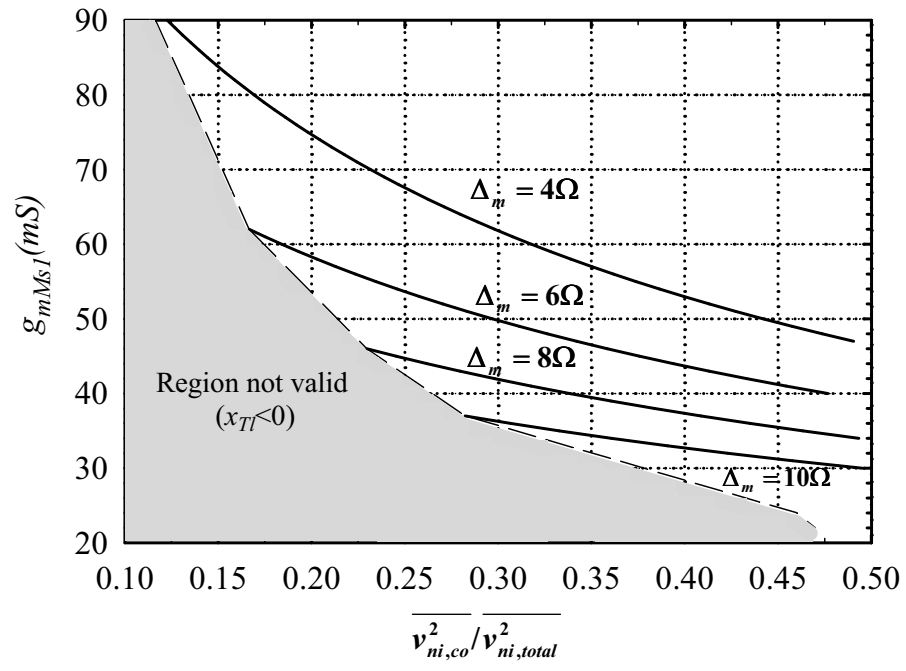


Fig. 81. Required $g_{m(Ms1)}$ versus the percentage contribution of additional tuning circuit for different input mismatch values ($NF_T = 3\text{dB}$, $\kappa\gamma = 2$).

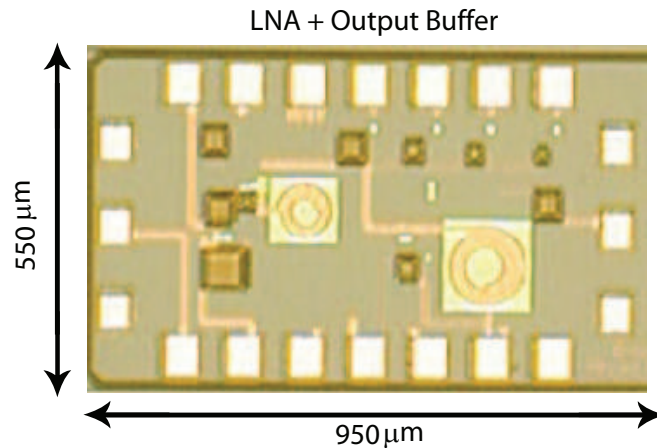


Fig. 82. Die micro photograph of the reconfigurable LNA.

E. Simulation and Experimental Results

The reconfigurable LNA is fabricated using $0.13\ \mu\text{m}$ CMOS technology provided through UMC. The chip is encapsulated in a QFN package for connecting the external components of the LNA including L_g . The RF signal is applied and monitored using on-wafer probing to reduce the losses and mismatches introduced by the measurement setup. The die micrograph is presented in Fig. 82, where the total area including the pads is $0.52\ \text{mm}^2$. The active area for the integrated devices and inductors is $0.083\ \text{mm}^2$. The effect of the output buffer is de-embedded from the LNA+Buffer measurements using the measurement results of a fabricated stand-alone buffer.

The complete schematic of the LNA including the external components, bonding and PCB parasitics is shown in Fig. 83. A buffer is added at the output of the LNA to drive the 50Ω input impedance of the network analyzer. The inductor L_{L2} is implemented using the wire bond inductance. The package and bonding effects are modeled by an LC network, and it is assumed that 1mm of bonding wire length

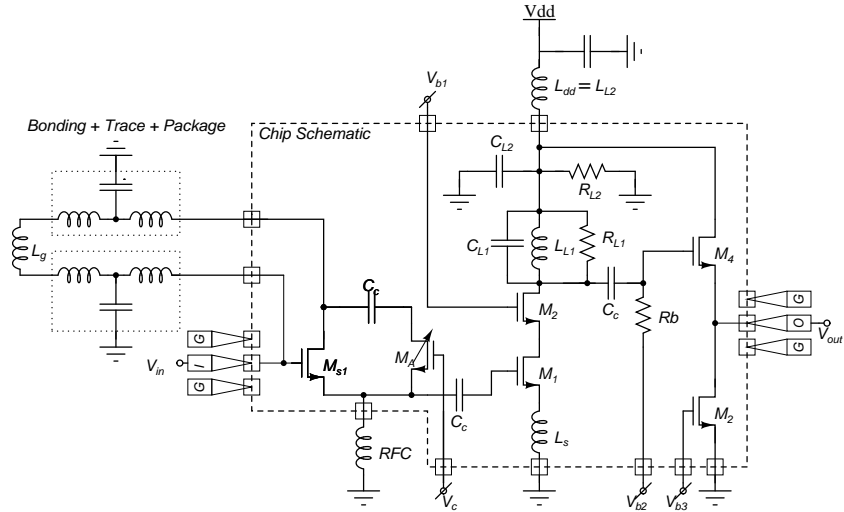


Fig. 83. PCB model of the measured LNA. The RF input and output signals are measured using the probes.

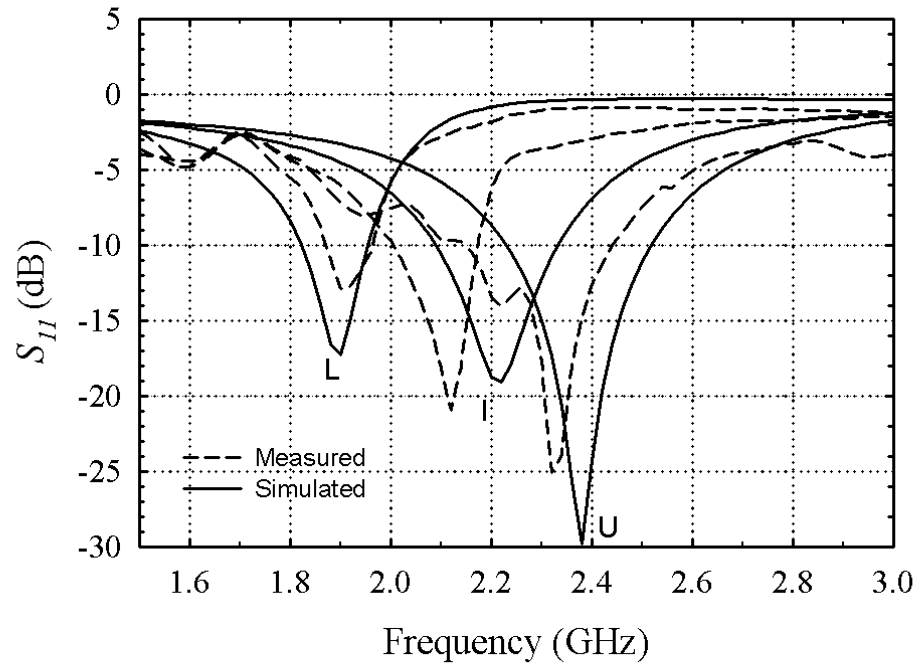


Fig. 84. Measured and simulated S_{11} of the reconfigurable LNA for different tuning frequencies. (L: lower band, I: intermediate band, U: upper band).

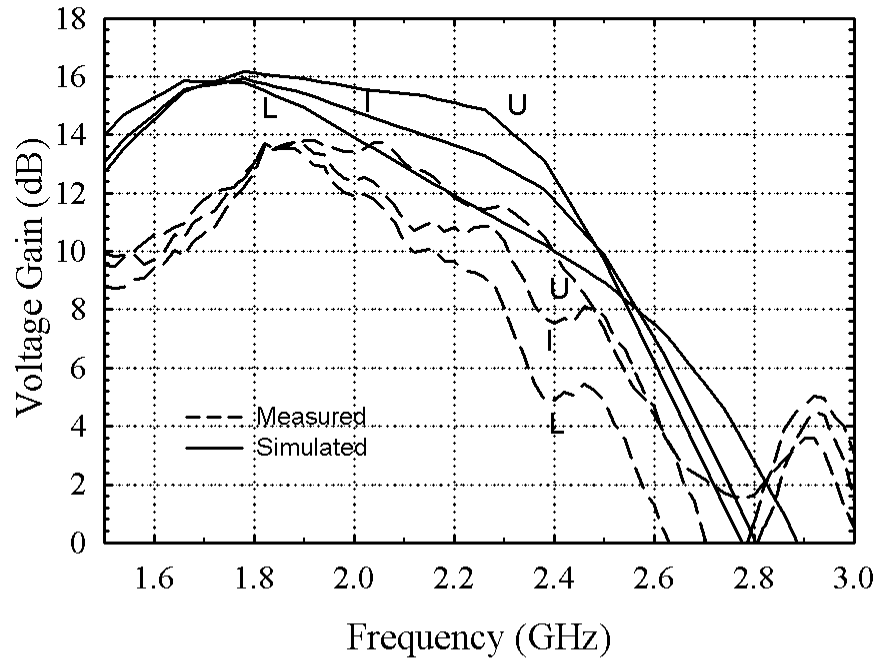


Fig. 85. Measured and simulated voltage gain versus the frequency (L: lower band, I: intermediate band, U: upper band).

is approximately 1 nH, and the pin capacitance is approximately 150 fF. An FR-4 PCB is used, and PCB traces are modeled using an equivalent LC circuit. Modeling the external components helps during the design phase to optimize the targeted performance after the measurement. The RF signals are applied and monitored using ground-signal-ground (GSG) RF probe to characterize the performance of the LNA.

The circuit S-parameters are measured using the HP8719ES network analyzer. Fig. 84 shows the measured and the simulated S_{11} , for different tuning frequencies. As noticed S_{11} is lower than -13 dB for the entire frequency range from 1.9 GHz to 2.4 GHz. This frequency range is suitable for the PCS standard at 1.9 GHz and various other standards at 2.4 GHz. The input tuning frequency is changed using the control voltage, V_c , which changes the equivalent resistance of the transistor M_A . As

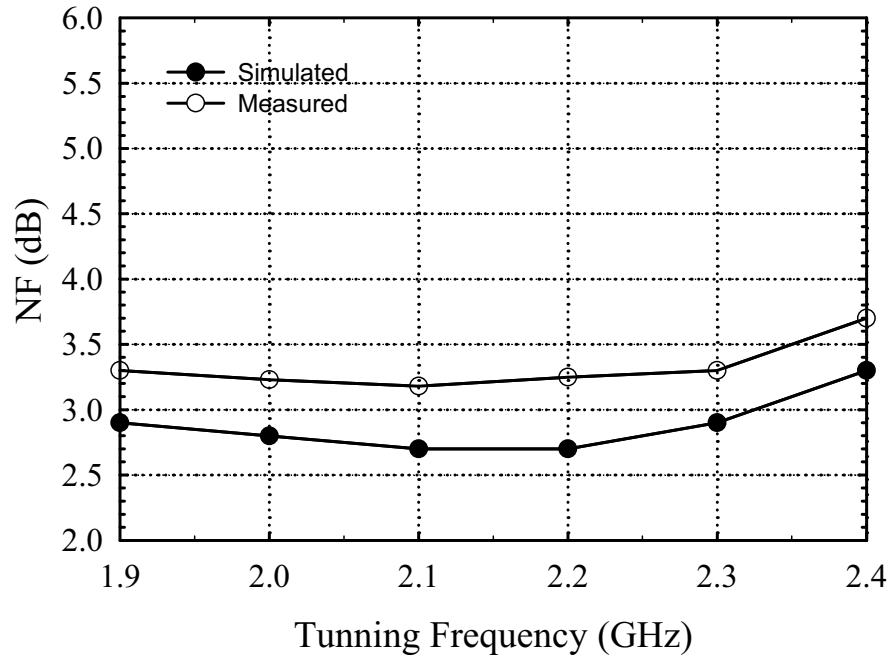


Fig. 86. Measured and Simulated Noise Figure versus the tuning frequency.

depicted from Fig. 84, the simulated and measured results matched over the same tuning range because of the accurate modeling of the PCB and bonding parasitics.

Fig. 85 shows the voltage gain after de-embedding the buffer effect. The measured voltage gain is between 10-14 dB for 1.9-2.4 GHz frequency bands. Both simulated and measured voltage gains have the same behavior, however the measured gain is about 2 dB lower than the simulated one. This difference could be due to the lower load resistance, R_{L1} , or transconductance, $g_{m(M1)}$, as a result of process variations.

The noise figure versus the tuning frequency is shown in Fig. 86, where the noise figure varies from 3.2 to 3.7 dB. The higher measured noise figure is mainly due to the lower gain of the LNA and the inaccuracy of the provided technology noise models. Having a tuned output load instead of the wideband one reduces the noise figure by 1 dB based on our simulation results. A two-tone IIP3 measurement is performed

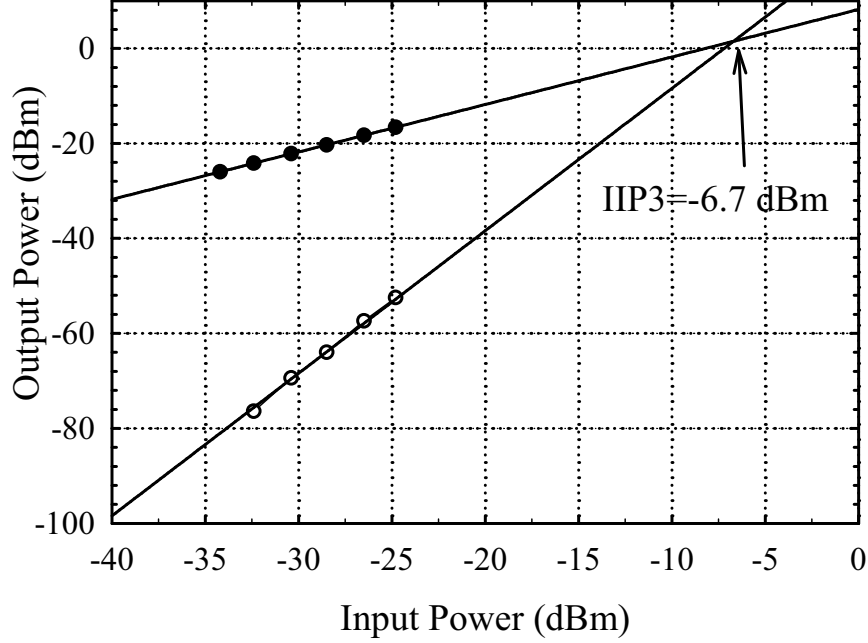


Fig. 87. Two-tone IIP3 measurement result ($f_o=2$ GHz).

for the LNA and the result is shown in Fig. 87 for f_o at 2 GHz. The two tones are applied with the same amplitude and a frequency offset of 10 MHz. The measured IIP3 is -6.7 dBm, and is limited by the transistor $M1$. The measurement shows that IIP3 is almost constant for the whole tuning range. The LNA consumes 14 mA from a 1.2 V supply. The main LNA section consumes 8 mA, and the additional circuitry for tuning L_g consumes 6 mA. The performance of the proposed LNA and comparison with the existing tunable architecture are summarized in Table X. As depicted in the table, the proposed reconfigurable LNA provides continuous tuning of the input matching network, while the other existing techniques either provide discrete tuning or wideband matching. The power consumption for the proposed architecture is higher when compared to [70] because an active circuit is used for tuning the inductor.

Table X. Performance summary of the proposed reconfigurable LNA and comparison with the existing work.

	Freq. Range (GHz)	Tuning	NF (dB)	V. Gain ³ (dB)	IIP3 (dBm)	V_{DD} (V)	P_{DC} (mW)	A. Area (mm ²)	Technology (CMOS)
Design 1:Measured	1.9 - 2.4	cont.	3.2 - 3.7	14 - 10	-6.7(@ 2GHz)	1.2	17	0.083 ⁴	0.13 μm
Design 2:Simulated	2.4 - 5.2	cont.	2 - 4.2	23 - 19	-3(@3 GHz)	1.2	17	0.083 ⁴	0.13 μm
[70]	0.9, 1.8 , 5.2	disc.	2.3 - 2.9	13 - 14	-14	1.8	7.5	N.A.	0.18 μm
[71] ²	1.8, 2.1 , 2.4	disc.	5.2 - 5.8	29	-7.5	1.2	20 - 24	0.6 ⁵	0.13 μm
[72]	0.75 - 2.5	cont.	4.8 - 10	24 - 28	-24	1.8	42	0.09	0.18 μm

¹ The output consists of a tuned resonator.

² LNA and Mixer measured performance.

³ Gain at the input tuned frequency.

⁴ L_g and RFC coils are external.

⁵ The area is estimated based on a total active area of 1.5 mm² and Fig. 7 in [71].

Also, two external RFC coils are used in the implementation.

To analyze another case, the circuit is designed for a wide tuning range with a reconfigurable load. Table X summarizes the performance summary for the post-layout simulated wide tuning range LNA. For this case, the output load is a resonant circuit, and the output tuning frequency is changed by means of a bank of capacitors and a varactor for coarse and fine tuning, respectively. This design example shows lower noise figure when compared to design 1, because the gain is higher and the noise contributed by the load resistance is lower. Design 2 demonstrates the extension of the proposed approach for wider tuning ranges to support various standards that appear in this frequency range. In addition, it is not easy to design a discrete input matching network that can provide this wide/fine-tuning range functionality.

F. Summary

A reconfigurable low noise amplifier (LNA) with continuous tuned input matching network was presented in this chapter. By means of an inductor tuning circuit, a tunable narrow-band LNA is obtained. The detailed analysis of the LNA, including the tuning range and additional noise of the proposed reconfigurable input matching network, was presented. In addition, a design methodology for minimizing the power consumption of the additional tuning circuit was proposed. This methodology was used to design and implement a reconfigurable LNA along the frequency band 1.9-2.4 GHz. The 0.13 μ m CMOS technology was used to implement the LNA, which consumes 14 mA from a 1.2 V supply. Measured performance shows an input matching better than -13 dB, a voltage gain of 10-14 dB, and a noise figure of 3.2-3.7 dB over the tuning range. In addition, post-layout simulations of a wide-tuning range LNA is also presented; the input matching network is tunable from 2.4 - 5.2 GHz. This work demonstrates the first technique for continuous tuning of the input match-

ing network. This technique results in multi-band LNAs that are smaller in area than either concurrent or switchable LNAs, and superior in performance to wide-band LNAs. In addition, the proposed technique is not only suitable for tuning the matching network, but can be generally used to scale the inductance value for any application.

CHAPTER V

LOW DROP-OUT REGULATOR WITH FEED-FORWARD RIPPLE CANCELLATION TECHNIQUE

Low drop-out (LDO) linear regulators is an important building block in power management ICs and usually comes after a DC-DC switching converter, as shown in Fig. 88. It is used to regulate the supplies ripples to provide a clean voltage source for the noise-sensitive analog/RF blocks. Designing a stable LDO for a wide range of load conditions, while achieving high power-supply-rejection (PSR), low drop-out voltage, and low quiescent current, is the main target using state-of-the-art CMOS technologies [73, 74, 75, 76].

Recently, there has been an increasing demand to integrate the whole power management system into a single system-on-chip (SoC) solution. Hence, operating frequencies of switching converters are increasing to allow higher level of integration [77]. This trend increases the frequency of output ripples and therefore the subsequent LDO regulator should provide high PSR up to switching frequencies. Conventional LDOs have poor PSR at high frequencies (above 300 kHz) especially the ones implemented using sub-250 nm technologies. The main reasons for poor PSR are summarized as follows: (1) Finite output conductance of the pass transistor, (2) low DC gain of sub-250 nm technologies which requires complex gain stages to achieve better regulation, and (3) finite bandwidth of the feedback path.

Researchers have contributed to improve power-supply-rejection techniques. Some of those techniques are: i) Using simple RC filtering at the output of the LDO [78]; ii) Cascading two regulators [78]; iii) Cascading another transistor with the PMOS pass transistor along with RC filtering, using special technologies such as drain-extended FET devices, and/or charge-pump techniques to bias the gate of one of the transis-

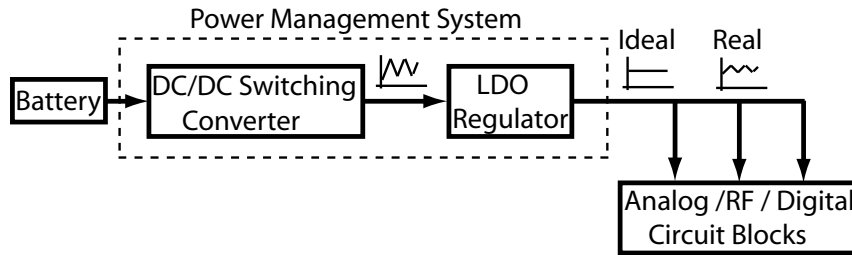


Fig. 88. Block diagram of typical power management system.

tors [16, 17, 79]. Simple RC filtering reduces the voltage ripple at the input of the LDO. However, this technique increases the drop-out voltage (reduces the efficiency) in LDO regulators that supply high current due to the high voltage drop across the resistance. Using an NMOS or PMOS transistor to cascade with the PMOS pass transistor can achieve high power-supply-rejection over a wide frequency range. This technique increases the area and leads to a high drop-out voltage (poor efficiency) [79]. Charge pump techniques increase complexity and lead to higher power consumption because a clock is necessary along with RC filtering to remove clock ripples [17]. In summary, the main idea behind all previously proposed techniques is to provide more isolation between the input and output along the high-current signal path. Hence, the area consumption and drop-out voltage are large, which is not suitable for low-voltage technologies. In addition, these techniques provide high PSR (input/output ripples) at low frequencies, but are unable to provide sufficient PSR (better than -50 dB) at frequencies up to several MHz.

To overcome the drawbacks of previously reported PSR LDO regulators, we introduce a high PSR low voltage LDO regulator based on a feed-forward ripple cancellation (FFRC) approach [23]. The proposed LDO topology preserves traditional loop dynamics structure, while providing high PSR over a wide frequency range. In

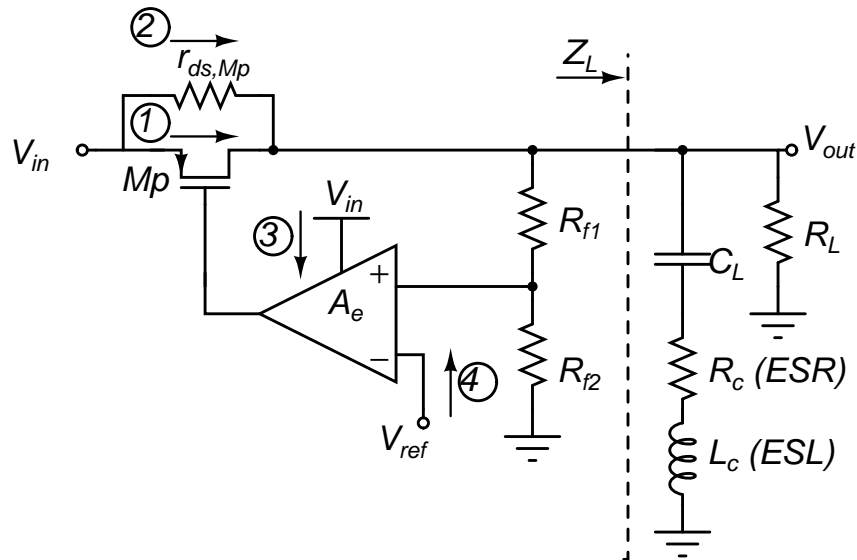


Fig. 89. Input to output ripple paths in conventional LDOs.

addition, it enables the design for high supply currents and low quiescent current consumption. This chapter is organized as follows: Section A discusses main *PSR* limitation sources in conventional LDOs. Section B presents the proposed FFRC-LDO. The stability analysis using a single bond-wire and a Kelvin connection are presented in section C. Section D demonstrates the circuit implementation. Measurement results are shown in Section E, and the summary is provided in section F.

A. *PSR* of Conventional LDOs

In this section, fundamental limitations for *PSR* improvement of conventional LDOs at high frequencies are investigated. It is shown that *PSR* at high frequencies is mainly limited by the dominant pole of the error amplifier and equivalent self inductance (ESL) and resistance (ESR) of the off-chip capacitor.

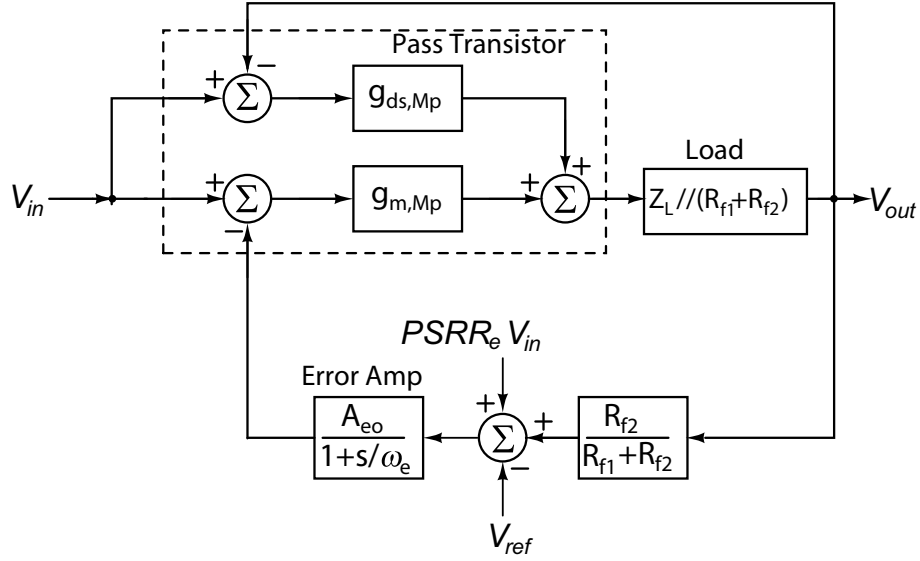


Fig. 90. Mathematical model of the conventional LDO.

The finite PSR of the conventional LDO is due to several paths between the input and output of the LDO. Fig. 89 shows various paths that could couple input ripples to the output of the LDO. Path 1 is the main path regulated by the LDO loop. Path 2 is caused by the finite conductance of the MOS pass transistor, M_p , and it is more significant for technologies with lower feature sizes. Path 3 is as a result of the finite power-supply-rejection ratio ($PSRR$) of the error amplifier, and finally path 4 is due to the finite PSR of the bandgap circuit.

The LDO transfer function due to paths 1 and 2 could be obtained with the help of Fig. 90 as follows

$$\frac{V_{out}}{V_{in}}(s)|_{1,2} = \frac{1 + g_{m,Mp} \cdot r_{ds,Mp}}{1 + \frac{r_{ds,Mp}}{Z_L(s)} + \frac{r_{ds,Mp}}{R_{f1} + R_{f2}} + \frac{g_{m,Mp} r_{ds,Mp} A_{eo} R_{f2}}{(R_{f1} + R_{f2})(1 + \frac{s}{\omega_e})}}. \quad (5.1)$$

where $g_{m,Mp}$ and $r_{ds,Mp}$ are the transconductance and channel resistance of the pass transistor, M_p . Z_L is the total load impedance (without feedback resistances R_{f1} and

R_{f2}) that appear at node V_{out} , and A_{eo} and ω_e are the DC gain and dominant pole of the error amplifier, respectively. Eq. (5.1) shows that PSR depends on the feedback gain ($A_{eo} \frac{R_{f2}}{R_{f1}+R_{f2}}$) at lower frequencies. For sub-250 nm technologies, increasing A_{eo} is challenging for conventional LDO designs.

As the frequency increases, the dominant pole of the error amplifier reduces the feedback gain; therefore, the PSR due to paths 1 and 2 starts to degrade as demonstrated by (5.1) from the term $\frac{A_{eo}}{1+s/\omega_e}$. Without considering ESL and ESR of the off-chip capacitor, $\frac{V_{out}}{V_{in}}|_{1,2}$ starts to decrease at higher frequencies because the off-chip capacitor shorts ripples to ground. However, due to ESL and ESR this effect does not happen at high frequencies, and the off-chip capacitor represents an open circuit. In this case, ripples at the output may get amplified at high frequencies. The upper and lower limits of PSR across the entire frequency spectrum due to paths 1 and 2 are given by

$$\begin{aligned} \frac{V_{out}}{V_{in}}(s=0)|_{1,2 \text{ lower}} &\approx \frac{1}{A_{eo} \frac{R_{f2}}{R_{f1}+R_{f2}}}, \\ \frac{V_{out}}{V_{in}}(s=\infty)|_{1,2 \text{ upper}} &\approx g_{m,Mp} \frac{R_L \cdot r_{ds,Mp}}{R_L + r_{ds,Mp}}. \end{aligned} \quad (5.2)$$

For paths 3 and 4, the transfer function is given by

$$\begin{aligned} \frac{V_{out}}{V_{in}}(s)|_{3,4} &= \frac{g_{m,Mp} \cdot Z_{tot}(s) \cdot \frac{A_{eo}}{1+\frac{s}{\omega_e}}}{1 + \frac{g_{m,Mp} \cdot Z_{tot}(s) \cdot A_{eo} R_{f2}}{(R_{f1}+R_{f2})(1+\frac{s}{\omega_e})}} (PSRR_e + PSR_{BG}), \\ Z_{tot}(s) &= Z_L(s) // r_{ds,Mp} // (R_{f1} + R_{f2}), \end{aligned} \quad (5.3)$$

where $PSRR_e$ is the power-supply-rejection ratio of the error amplifier, and PSR_{BG} is the power-supply-rejection of the bandgap circuit. Eq. (5.3) shows that the finite PSR due to paths 3 and 4 is an amplified quantity of $PSRR_e$ and PSR_{BG} . The amplification is given by the ratio of feedback resistances as $1 + \frac{R_{f1}}{R_{f2}}$. At higher frequencies due to the dominant pole of error amplifier, $\frac{V_{out}}{V_{in}}|_{3,4}$ goes to zero, and

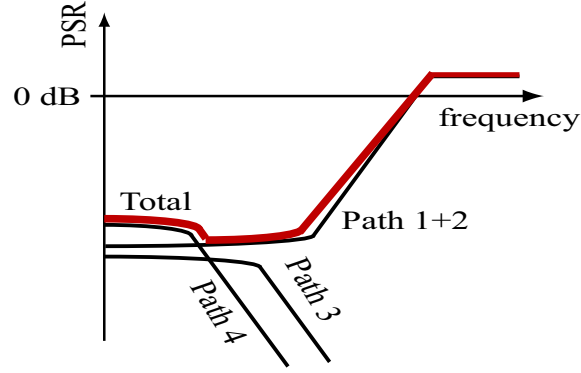


Fig. 91. Total PSR of LDO and PSR due each path in Fig. 89.

hence, ripples leaking through the error amplifier and bandgap do not appear at the output.

In summary, all four paths affect the PSR at low frequencies and only paths 1 and 2 affect the PSR at high frequencies. Fig. 91 demonstrates the effect of each path on the overall PSR of the conventional LDO. Several techniques could be applied to reduce the PSR at lower frequencies by decreasing $PSRR_e$, PSR_{BG} and increasing gain of error amplifier. However at higher frequencies, the dominant pole of the error amplifier degrades the PSR of the LDO, and the off-chip capacitor is considered as an open circuit because of its ESL. None of the previously presented techniques have solved this problem satisfactorily. Usually, the PSR of LDO starts to degrade around 10-100 kHz [17]. A proposed solution for achieving high PSR at higher frequencies is demonstrated in the next section.

B. Proposed Feed-Forward Ripple Cancellation LDO

The PSR at low frequencies can be enhanced by increasing the feedback gain of the LDO. However at high frequencies, the PSR is mainly due to paths 1 and 2 in

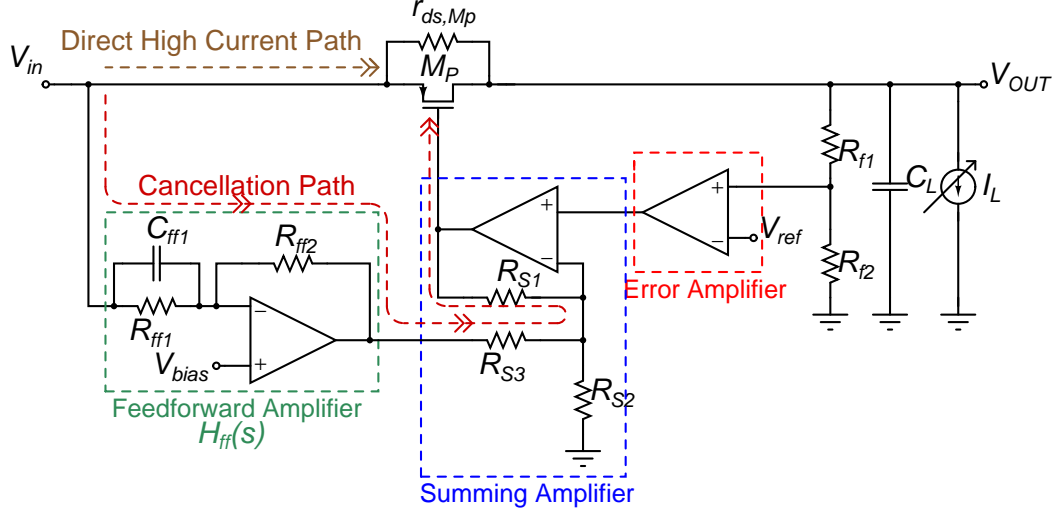


Fig. 92. Block-level representation of the feed-forward ripple cancellation LDO (FFR-C-LDO).

Fig. 89, and is limited by the dominant pole of the feedback loop. To achieve higher PSR at both DC and high frequencies, ripples generated in paths 1 and 2 should be removed. The basic idea of the proposed LDO is demonstrated below. Its sensitivity to process-temperature (PT) variations is also discussed.

1. Basic Idea

To eliminate input ripples from appearing at the output, a zero transfer gain is necessary from the input to the output in Fig. 89. In the ideal case (without considering $r_{ds,Mp}$), this is achieved by implementing a feed-forward path that replicates same input ripples at the gate of the pass transistor. Hence, the gate-overdrive voltage is independent of input ripples, and as a result no ripple appears across the load. In the actual case (with $r_{ds,Mp}$), part of the ripples leak through the finite output resistance of M_p , and should be removed. This is done by increasing the ripple amplitude appearing at the gate of M_p to cancel ripples that leak through $r_{ds,Mp}$ by an amount

of $(g_{m,Mp} + g_{ds,Mp})/g_{m,Mp} = 1 + 1/A_{v,p}$, where $A_{v,p}$ is the inherent voltage gain of the pass transistor.

Fig. 92 presents a simplified block-level description of the proposed FFRC-LDO. Supply ripples, appearing at the source of pass transistor M_p , are reproduced at the gate of M_p using the feed-forward path. The generated ripples at the gate are higher in magnitude than input ripples to cancel additional ripples appearing at the output due to $r_{ds,Mp}$ (path 2 in Fig. 89). The feed-forward path is implemented using a feed-forward amplifier and a summing amplifier. The summing amplifier is used to merge the feedback regulating loop with feed-forward path at the gate of the transistor M_p .

Optimum value of the feed-forward gain is obtained with the help of a mathematical model of the FFRC-LDO, as shown in Fig. 93. Without the feed-forward path, $H_{ff}(s)$, the mathematical model is equivalent to a conventional LDO. The transfer gain of the system involving $H_{ff}(s)$ yields

$$\frac{V_{out}}{V_{in}}(s) = \frac{1 + \frac{g_{m,Mp}}{g_{ds,Mp}} \cdot [1 - H_{ff}(s) \frac{A_{so}}{1 + \frac{s}{\omega_s}}]}{1 + \frac{1}{g_{ds,Mp} \cdot Z_L(s)} + \frac{1}{g_{ds,Mp} \cdot (R_{f1} + R_{f2})} + \frac{g_{m,Mp}/g_{ds,Mp} \cdot A_{eo} R_{f2}}{(R_{f1} + R_{f2})(1 + \frac{s}{\omega_e})}}. \quad (5.4)$$

where A_{so} and ω_s are the DC gain and dominant pole of the summing amplifier, respectively. To remove the ripples at the output, (5.4) should be set to be zero. Hence, the optimum value for the feed-forward amplifier, $H_{ff}(s)|_{opt}$, is then given by

$$\begin{aligned} H_{ff}(s)|_{opt} &= \frac{1 + \frac{s}{\omega_s}}{A_{so}} \cdot \left(1 + \frac{g_{ds,Mp}}{g_{m,Mp}}\right) \\ &= \frac{1 + \frac{s}{\omega_s}}{A_{so}} \cdot \left(1 + \frac{1}{A_{v,p}}\right). \end{aligned} \quad (5.5)$$

Eq. (5.5) demonstrates that the optimum feed-forward gain has to contain a zero in its transfer function. The zero cancels the effect of the pole existing at the gate of the pass transistor to extend the frequency range of the ripple rejection. Hence, this

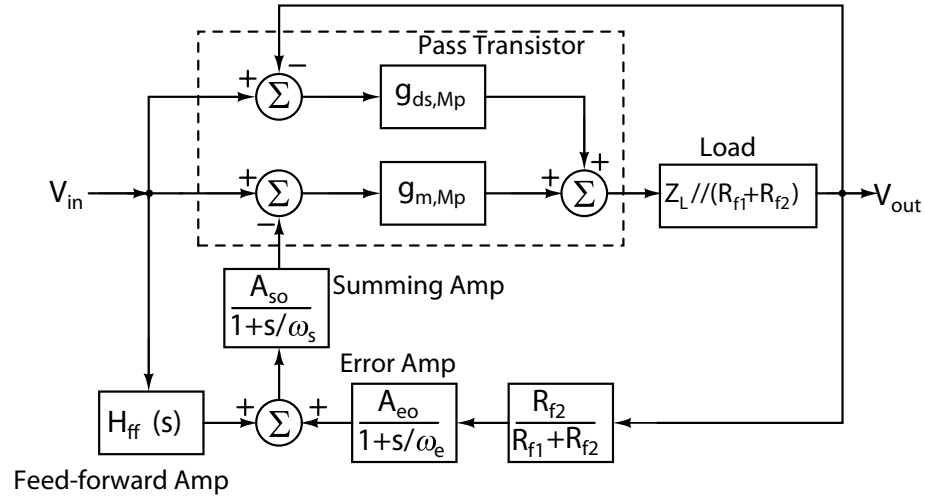


Fig. 93. Mathematical model of the FFRC-LDO.

cancellation technique is limited by internal poles of the summing and feed-forward amplifiers. The zero is implemented using the capacitor C_{ff1} and resistor R_{ff1} in Fig. 92.

The simulated PSR of the LDO with and without FFRC technique is demonstrated in Fig. 94. Using the conventional architecture, the achieved PSR is less than 60 dB and it starts to degrade around 330 kHz. This frequency is located at the dominant pole of the error amplifier. Using the FFRC-LDO the PSR at DC is enhanced by 20 dB. Besides, the additional zero increases the frequency at which the PSR starts to increase to 9 MHz. This simulation shows the effectiveness of the FFRC-LDO to enhance the PSR at both DC and high frequencies. The PSR starts initially to increase around 330 kHz, which is the bandwidth of the error amplifier. Then around 1 MHz, the introduced zero stops the increase in the PSR . Due to the self-resonance frequency of the off-chip capacitor and finite non-dominate poles of the feed-forward and summing amplifiers, the PSR starts to degrade again at high

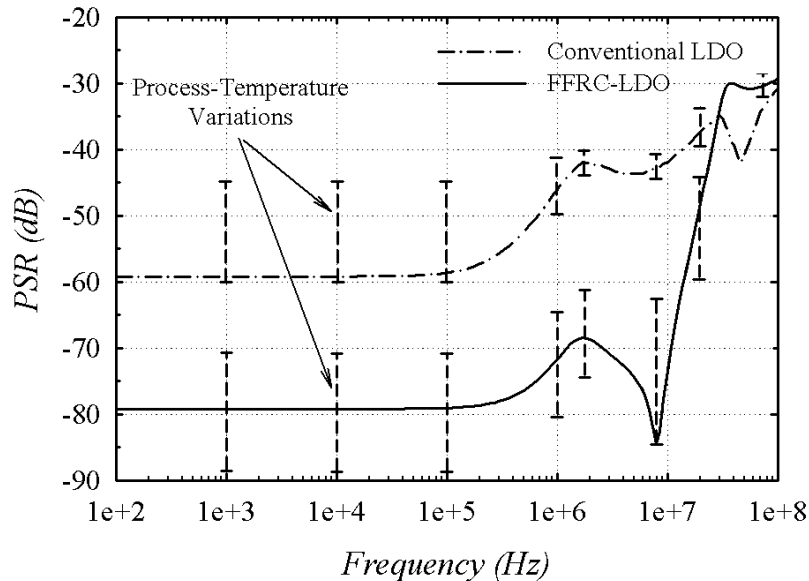


Fig. 94. *PSR* schematic simulations of conventional and FFRC-LDO ($R_L = 40 \, \Omega$). The effect of PT variations are also demonstrated.

frequencies. The main advantage of this FFRC approach is achieving a high *PSR* for a wide frequency range, without the need to increase the loop bandwidth and hence the quiescent power consumption. Moreover, this approach preserves the same low drop-out voltage of a conventional regulator, since supply rejection does not occur on the high-current signal path. The gain of the feed-forward and summing amplifiers is based on the ratio of resistors to reduce its dependency to process-temperature (PT) variations. Fig. 94 also shows the simulated variations of *PSR* of the FFRC-LDO for a temperature ranging from -40 to $125 \, ^\circ\text{C}$, and across process corners. Simulations over PT variations indicate that the LDO achieves comparable performance to that measured in the lab, making the LDO robust for high-performance power management ICs.

The variation of the *PSR* versus the load current is shown in Fig. 95. As depicted, the *PSR* has its best value for a current of $5 \, \text{mA}$ at low frequencies. As the current

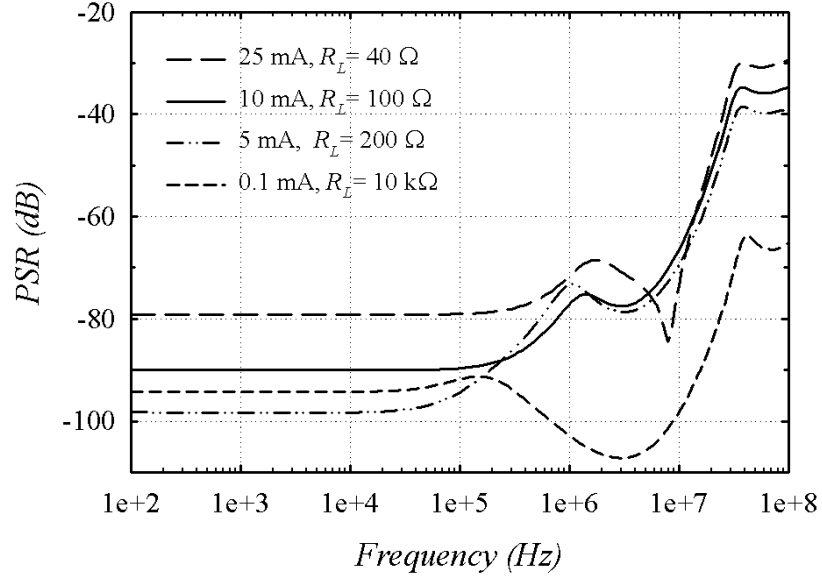


Fig. 95. *PSR* schematic simulations of FFRC-LDO for various load conditions ($R_L = 40, 100, 200, 10000 \Omega$).

increases, *PSR* is degraded due to the dependency of the DC gain of M_p ($g_{m,Mp} \cdot r_{ds,Mp}$) on the output current as given by (5.5). In this design, the optimum H_{ff} is selected to provide perfect cancellation at a load current of 5 mA. For small currents, the transistor M_p is biased in deep saturation with a DC gain of 20 dB. As the current increases, the transistor operating point moves near the linear region, and therefore, the DC gain is reduced to 14 dB at a load current of 25 mA. This example shows that $H_{ff}(s)$ has to be configurable if the LDO is designed to cover a wide range of currents. To increase the *PSR* at higher current, the drop-out voltage should increase such that the DC gain is higher.

The biasing voltage of the summing amplifier, V_{bias} in Fig. 92 has to be adjusted such that the output DC voltage of the summing amplifier is higher than zero, i.e.

$$V_{bias} \cdot \left(1 + \frac{R_{ff2}}{R_{ff1}}\right) - V_{in} \cdot \frac{R_{ff2}}{R_{ff1}} > 0. \quad (5.6)$$

As a result, there is a minimum value for V_{bias} for proper operation of the FFRC-LDO. $V_{bias}|_{min}$ is given by

$$V_{bias}|_{min} = V_{in}|_{max} \cdot \frac{R_{ff2}}{R_{ff1} + R_{ff2}}. \quad (5.7)$$

As high PSR is only required when the output is stabilized, this system biases the positive terminal of the feed-forward amplifier directly from the output, i.e. $V_{bias} = V_{out}$. The maximum input voltage that can be applied in this case is 2 V for an output voltage of 1 V and $R_{ff2}/R_{ff1} = 1$. Connecting the output directly to V_{bias} requires no additional voltage reference circuit. However, in a different design, another reference voltage can be added if the output voltage of the LDO is not high enough to satisfy the condition in (5.7).

2. Effect of Finite $PSRR$ of Summing and Feed-forward Amplifiers

The effect of finite $PSRR$ of summing and feed-forward amplifiers is studied in this section. It will be demonstrated that the PSR performance of these two amplifiers do not affect the PSR of the LDO significantly.

a. Feed-forward Amplifier

The finite PSR of an amplifier can be modeled as an additive voltage at its output as shown in the equivalent model in Fig. 96(a). Usually, for two stage amplifier PSR is higher than 0 dB, and therefore two stage amplifiers are characterized by their poor PSR . However, connecting feedback resistances (R_{ff1} and R_{ff2}) helps to reduce the effective PSR of the feed-forward amplifier by the loop gain. With the help of the equivalent model in Fig. 96(b), the output voltage, $v_{psr,ff}$, that appears due to the

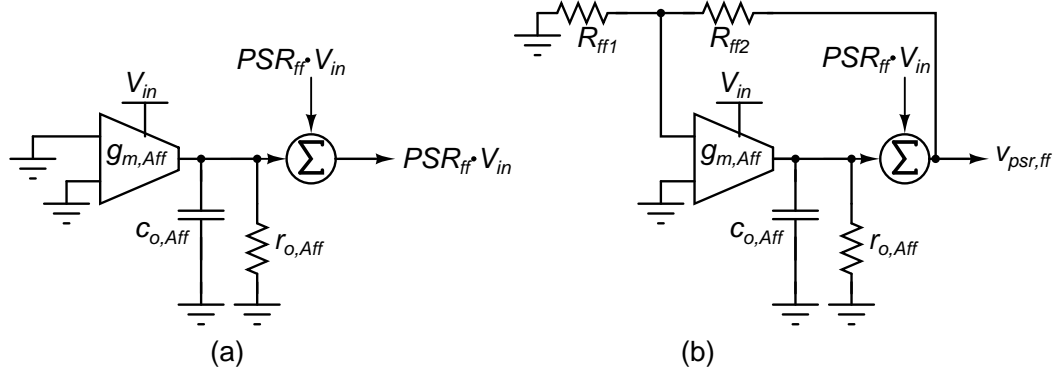


Fig. 96. Modeling of finite PSR of feed-forward amplifier (a) without feedback connection (b) with feed-back connection.

finite PSR of the amplifier is given by

$$\frac{v_{psr,ff}}{V_{in}} = PSR_{ff} \cdot \frac{R_{ff1} + R_{ff2}}{G_{ff} \cdot R_{ff1}}. \quad (5.8)$$

where PSR_{ff} is the power supply rejection of the feed-forward amplifier without the feedback connection, and $G_{ff} = g_{m,Aff} \cdot r_{o,Aff}$ is the open loop gain of the feed-forward amplifier. In our design, $PSR_{ff} = 3$ dB and loop gain $\frac{R_{ff1} + R_{ff2}}{G_{ff} \cdot R_{ff1}}$ is 38 dB. Hence, $\frac{v_{psr,ff}}{V_{in}} = -35$ dB. The voltage $v_{psr,ff}$ can be modeled as an additive at the output of the amplifier in Fig. 93.

Considering only the effect of $v_{psr,ff}$, on the supply rejection of the LDO, the output PSR of the whole LDO, $PSR_{vout,ff}$, due to the feed-forward amplifier is obtained by dividing (5.8) by the feedback gain of the LDO ($\frac{A_{eo} \frac{R_{f2}}{R_{f1} + R_{f2}}}{1 + \frac{s}{\omega_e}}$), resulting in

$$PSR_{vout,ff} \approx PSR_{ff} \cdot \frac{R_{ff1} + R_{ff2}}{G_{ff} \cdot R_{ff1}} \cdot \frac{1 + \frac{s}{\omega_e}}{A_{eo} \frac{R_{f2}}{R_{f1} + R_{f2}}}. \quad (5.9)$$

Equation (5.9) shows that the poor PSR of the feed-forward amplifier is attenuated by feedback resistances and the gain of error amplifier. Combining all these

effects, $PSR_{vout,ff}$ is about 93 dB in the designed FFRC LDO.

b. Summing Amplifier

Similar to the feed-forward amplifier, the poor PSR of the summing amplifier is reduced through its loop gain. This effect is also modeled as an additive voltage, $v_{psr,ff}$, at the output of the amplifier that is given by

$$\frac{v_{psr,ss}}{V_{in}} = PSR_{ss} \cdot \frac{R_{s2}/R_{s3} + R_{s1}}{G_{ss} \cdot R_{s2}/R_{s3}}. \quad (5.10)$$

where PSR_{ss} is the power supply rejection of the summing amplifier without the feedback connection, and G_{ss} is the gain of the summing amplifier without the feedback connection. The output PSR of the whole LDO, $PSR_{vout,ss}$, due to the finite PSR of the summing amplifier is given by

$$PSR_{vout,ss} \approx -PSR_{ss} \cdot \frac{R_{s2}/R_{s3} + R_{s1}}{G_{ss} \cdot R_{s2}/R_{s3}} \cdot \frac{1 + \frac{s}{\omega_e}}{A_{eo} \frac{R_{f2}}{R_{f1} + R_{f2}}} \cdot \frac{1 + \frac{s}{\omega_s}}{A_{so}}. \quad (5.11)$$

Equation (5.11) shows that the finite PSR of the summing amplifier is attenuated by its loop gain, error amplifier gain, and the summing amplifier gain. Simulations show a $PSR_{vout,ss}$ higher than 95 dB is achievable.

In summary, the above analysis showed that the finite PSR of the feed-forward and summing amplifier can be neglected in the analysis as stated earlier in this section.

C. Stability Analysis

In this section, the design of a stable LDO is demonstrated. Ideally, the feed-forward path does not affect the stability of the LDO because it does not exist in the feedback loop. However in this implementation, the node V_{bias} of feed-forward amplifier is connected to V_{out} to remove the need for another reference voltage. Hence, the feed-

forward path appears in the feedback, but still it does not affect the stability as demonstrated in this section. The effect of packaging is considered to highlight the importance of considering the inductance of the bond wire. Two cases are considered: (1) A single bond-wire and (2) a Kelvin connection (two bond-wires).

1. Single Bond-Wire

Fig. 97 shows the open loop circuit diagram of the proposed LDO when a single bond wire is used to interface with the external components. The equivalent series inductance (ESL) and resistance (ESR) of the off-chip capacitor is also considered in the analysis. The open loop gain of the LDO is given by

$$\begin{aligned} \frac{v_{x,o}}{v_{x,i}} &= \frac{v_g}{v_{x,i}} \cdot \frac{i_p}{v_g} \cdot \frac{v_{x,o}}{i_p} = - \frac{g_{m,Mp}}{\left(1 + \frac{s c_{o,As} \left(1 + \frac{R_{s1}}{R_{s2} // R_{s3}}\right)}{g_{m,As}}\right)} \cdot (A_{fb} - A_{ff}) \cdot \frac{v_{x,o}}{i_p}, \quad (5.12) \\ A_{fb} &= \frac{R_{f2} g_{m,Ae} r_{o,Ae} \left(1 + \frac{R_{s1}}{R_{s2} // R_{s3}}\right)}{(R_{f1} + R_{f2}) (1 + s r_{o,Ae} c_{o,Ae})}, \\ A_{ff} &= \frac{R_{s1} \left(1 + \frac{R_{ff2}}{R_{ff1}}\right) (1 + s C_{ff1} (R_{ff1} // R_{ff2}))}{R_{s3}}, \end{aligned}$$

where $v_{x,o}$, $v_{x,i}$, v_g , and i_p are as shown in Fig. 97, $g_{m,Ae}$, $g_{m,As}$, and $g_{m,Mp}$ are the effective transconductance of error amplifier, summing amplifier, and pass transistor, respectively, and $r_{o,Ae}$ and $c_{o,Ae}$ are the total resistance and capacitance at the output of error amplifier. Also, $r_{o,As}$ and $c_{o,As}$ are the total resistance and capacitance at the output of summing amplifier. A_{fb} is the gain of the error amplifier, and A_{ff} is the additional term due to connecting V_{bias} of the feed-forward amplifier to V_{out} . A_{ff} does not affect the stability of the LDO because it is much smaller than A_{fb} , and the loop bandwidth is determined by the output pole. Fig. 98 shows stability simulation results of the LDO when V_{bias} is connected to V_{out} and when it is connected to a

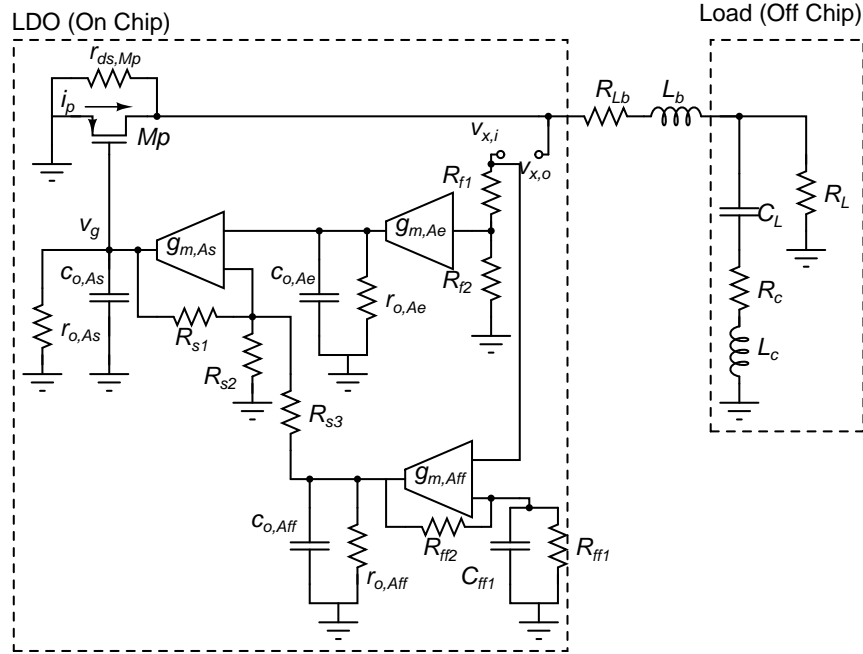


Fig. 97. Open loop equivalent circuit with single bond wire connection.

constant reference voltage. As depicted, the feed-forward path does not affect the stability of LDO even if V_{bias} is connected to V_{out} .

The term $\frac{v_{x,o}}{i_p}$ in (5.12) is the one that is different in single bond wire case and Kelvin connection case. For the single bond wire case, $\frac{v_{x,o}}{i_p}|_{single}$ is given by

$$\begin{aligned}
 \frac{v_{x,o}}{i_p}|_{single} &\approx R_{tot} \cdot \frac{1 + \frac{s}{Q_{z,s}} \frac{1}{\omega_{oz,s}} + \frac{s^2}{\omega_{oz,s}^2}}{\left(1 + \frac{s}{\omega_{pL1}}\right) \left(1 + \frac{s}{\omega_{pL2}}\right)} \\
 &\approx R_{tot} \cdot \frac{1 + \frac{s}{Q_{z,s}} \frac{1}{\omega_{oz,s}} + \frac{s^2}{\omega_{oz,s}^2}}{\left(1 + \frac{s}{\omega_{pL1}}\right)}, \\
 Q_{z,s} &= \frac{\sqrt{(L_b + L_c) C_L}}{\left(\frac{L_b}{R_L} + C_L (R_c + R_{Lb})\right)},
 \end{aligned} \tag{5.13}$$

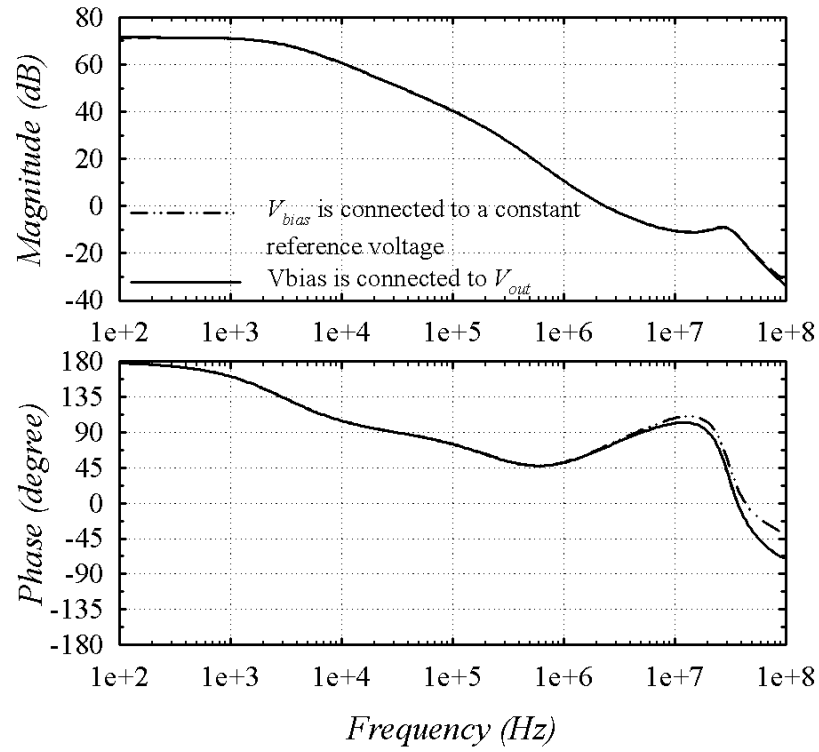


Fig. 98. Schematic simulations of the open loop gain and phase frequency responses when V_{bias} is connected to V_{out} or to a constant reference voltage ($L_b=0$ nH, $C_L = 4 \mu\text{F}$, $L_c = 0.4$ nH, $R_c = 30$ m Ω , $R_L = 40 \Omega$, $R_{tot} = 14 \Omega$).

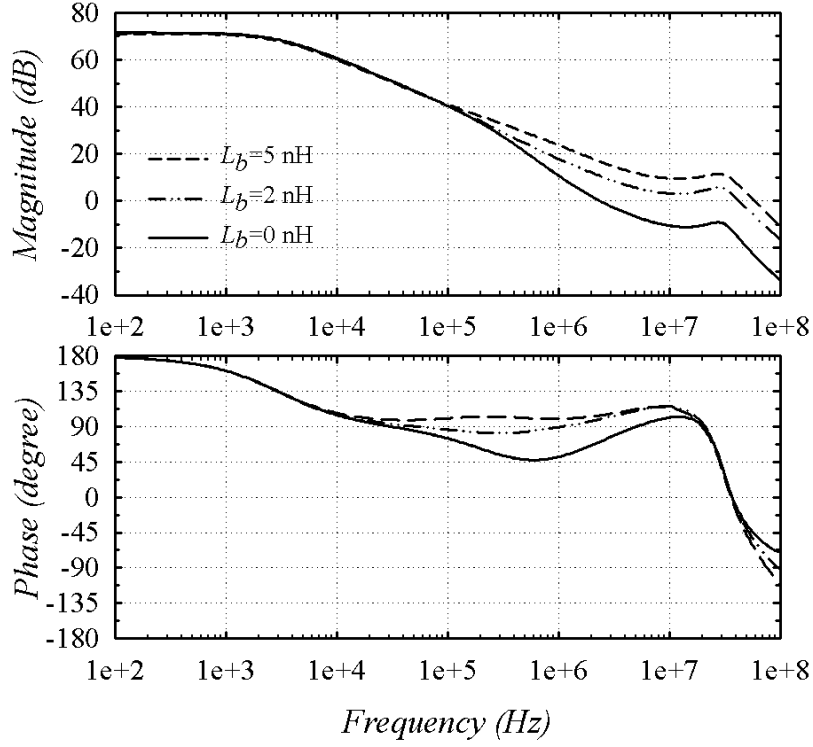


Fig. 99. Schematic simulations of the open loop gain and phase frequency responses for different values of L_b using single bond-wire ($C_L = 4 \mu\text{F}$, $L_c = 0.4 \text{ nH}$, $R_{Lb} = 40 \text{ m}\Omega$ per 1 nH , $R_c = 30 \text{ m}\Omega$, $R_L = 40 \Omega$, $R_{tot} = 14 \Omega$).

$$\begin{aligned}\omega_{oz,s} &= \frac{1}{\sqrt{(L_b + L_c) C_L}}, \\ \omega_{pL1} &= \frac{1}{C_L R_{tot}}, \\ \omega_{pL2} &= \frac{R_{tot}}{L_c + L_b \frac{R_{tot}}{r_{ds,Mp} // (R_{f1} + R_{f2})}}, \\ R_{tot} &= R_L // r_{ds,Mp} // (R_{f1} + R_{f2}).\end{aligned}$$

where R_{Lb} is the series resistance of the bond-wire.

Eqs. (5.12) and (5.13) show that the open loop transfer function consists of four

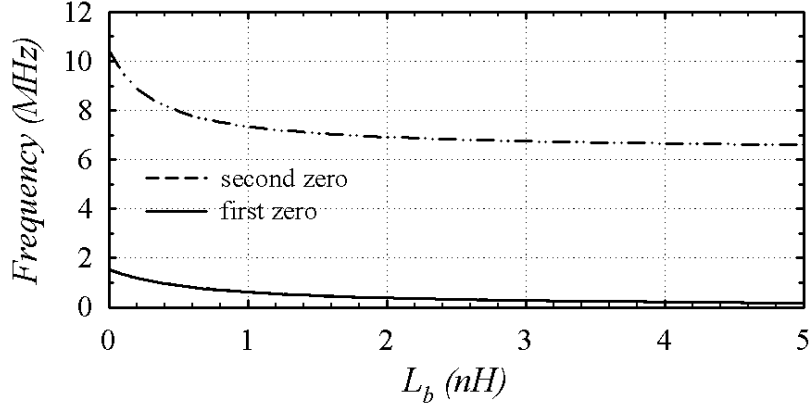


Fig. 100. Zero locations of $\frac{v_{x,o}}{i_p}|_{single}$ for different values of L_b ($C_L = 4 \mu\text{F}$, $L_c = 0.4 \text{ nH}$, $R_{Lb} = 40 \text{ m}\Omega$ per 1 nH , $R_c = 30 \text{ m}\Omega$, $R_L = 40 \Omega$, $R_{tot} = 14 \Omega$).

poles and two zeros. ω_{pL1} is the dominant pole of the loop. ω_{pL2} can be neglected because it appears at very high frequency (GHz range). The other two poles in (5.12) are the first two non-dominant poles. If L_b and L_c are neglected, only one real zero ($\frac{1}{C_L R_c}$) appears and is used to cancel the first non-dominant pole ($\frac{1}{r_{o,Ae} C_{o,Ae}}$ in this case). However in the practical case, L_b and L_c have values of at least 2 and 0.4 nH, respectively. These finite values produce two zeros. Increasing the value of L_b reduces the value at which these two zeros appear. The simulated frequency response for different values of L_b , while $L_c=0.4 \text{ nH}$, is shown in Fig. 99. As depicted, increasing L_b beyond a specific value may lead to an instability of the LDO.

The main reason for the instability is that higher values of L_b reduce the value of $\omega_{oz,s}$, and hence, the two zeros move to a lower frequency. Fig. 100 shows zero locations of (5.13) for different values of L_b . For $L_b = 0$, the first zero cancels the first non-dominant pole by adjusting the value of R_c , and the second zero appears above the gain-crossover frequency. As L_b increases, two zeros start to move towards DC, and as a result, the gain-crossover frequency is located at higher frequencies.

This situation lead to instability of the LDO because the higher non-dominant poles change the phase abruptly at higher frequencies (Fig. 99). To solve this problem, the dominant pole should be decreased to a lower frequency to guarantee the second zero is located after the gain-crossover frequency. As a result, increasing L_b requires reducing the gain-bandwidth product (GBW), and hence the speed of the LDO, when the zero (due to ESR) is used to compensate any non-dominate pole. This example shows the locations of zeros are very sensitive to L_b , and it may affect the functionality of LDO.

In summary, the disadvantage of using a single bond-wire can be summarized as follows: (1) zeros are sensitive to the value of L_b , (2) the loop bandwidth has to be decreased, hence lowering the speed, and (3) there is a voltage drop across the bond-wire due to its series resistance which affects the load regulation. Kelvin connection solves these issues.

2. Kelvin Connection

To remove the dependency of the two zeros in (5.13) to L_b , a Kelvin connection is used as an interface with the external load (Fig. 101). The Kelvin connection relies on closing the loop using two bond wires that are connected to the same pin of the package. In this case, $\frac{v_{x,o}}{i_p}|_{kelvin}$ is given by

$$\begin{aligned} \frac{v_{x,o}}{i_p}|_{kelvin} &\approx R_{tot} \cdot \frac{1 + \frac{s}{Q_{z,k}\omega_{oz,k}} + \frac{s^2}{\omega_{oz,k}^2}}{\left(1 + \frac{s}{\omega_{pL1}}\right)\left(1 + \frac{s}{\omega_{pL2}}\right)}, \\ Q_{z,k} &= \sqrt{\frac{L_c}{C_L}} \cdot \frac{1}{R_c}, \\ \omega_{oz,k} &= \frac{1}{\sqrt{L_c C_L}}. \end{aligned} \tag{5.14}$$

Eq. (5.14) shows that the zeros in $\frac{v_{x,o}}{i_p}|_{kelvin}$ do not depend on L_b , and hence a

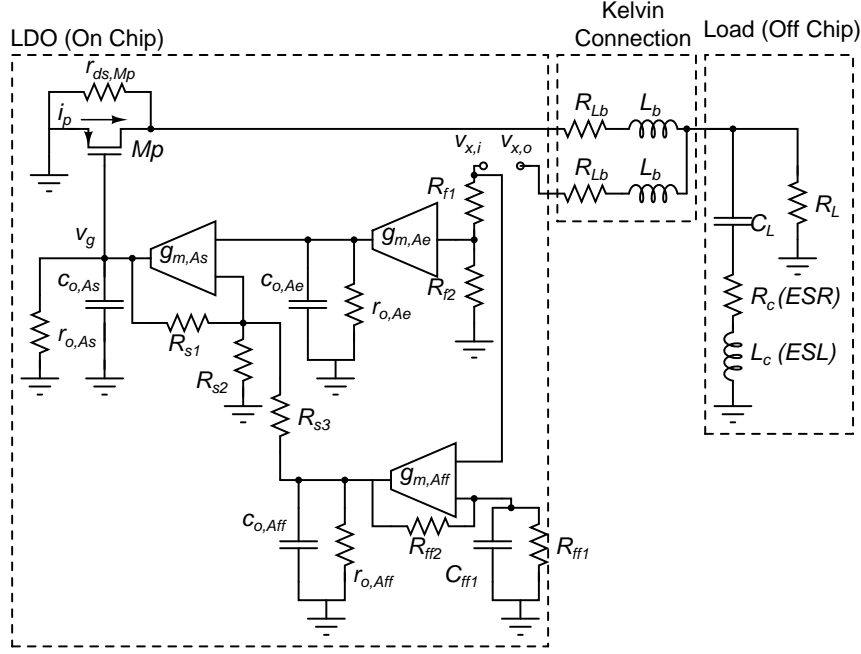


Fig. 101. Open loop equivalent circuit with a Kelvin connection.

more robust design can be implemented. The zero produced using the ESR of off-chip capacitor, R_c , can be used to compensate the first non-dominant pole, as a result allowing for a larger GBW product. Fig. 102 shows the simulated open loop gain of the proposed LDO using a Kelvin connection for different values of L_b . As depicted, the magnitude response does not change significantly with L_b when compared to a single bond-wire case. Hence, the design of a more stable LDO system is feasible using the Kelvin connection.

The simulated open-loop transfer function of the LDO schematic using a Kelvin connection is shown in Fig. 103. For heavy load condition ($R_L = 40 \Omega$), the LDO achieves a phase margin of 68° with a GBW of 2 MHz. The first non-dominant pole is due to the error amplifier ($\frac{1}{r_{o,Ae} \cdot C_{o,Ae}}$) and appears at 330 kHz. This pole is compensated using the real zero produced by ESR of the capacitor. The pole at the

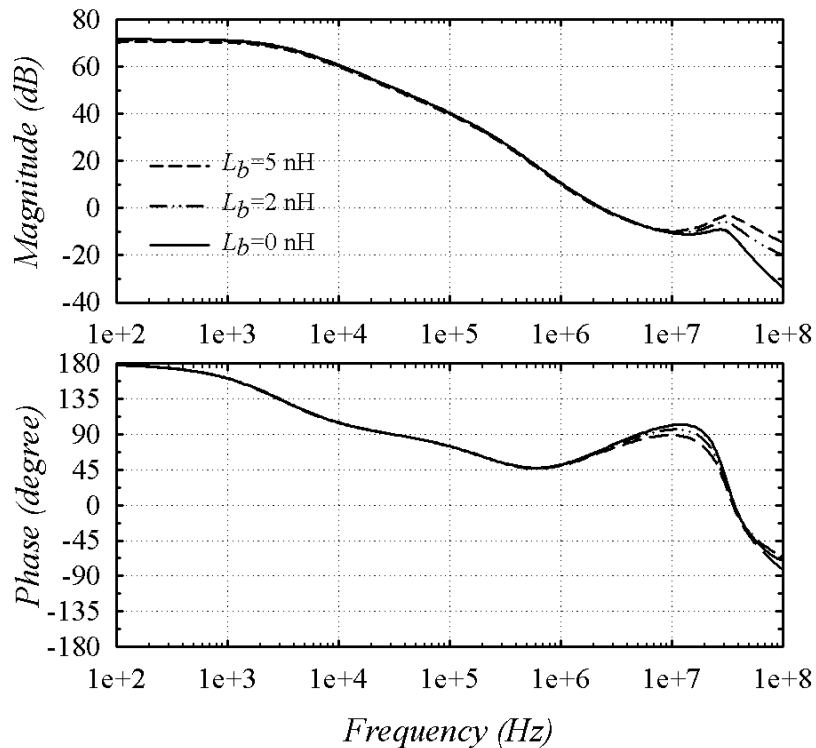


Fig. 102. Schematic simulations of the open loop gain and phase frequency responses for different values of L_b using Kelvin connection ($C_L = 4 \mu\text{F}$, $L_c = 0.4$ nH, $R_{Lb} = 40$ m Ω per 1 nH, $R_c = 30$ m Ω , $R_L = 40$ Ω , $R_{tot} = 14$ Ω).

gate of the pass transistor appears at a much higher frequency because of the small output resistance of summing amplifier and the use of smaller technology that reduces the node capacitance.

For the light load condition ($R_L = 10$ k Ω) a GBW of 110 kHz with a phase margin of 73° is obtained (Fig. 103). An important observation in Fig. 103 is the complex poles that result in peaking after the unity gain frequency. In case of a single wire, this peaking crosses 0 dB leading to instability. However using the Kelvin connection, the peaking amplitude has been reduced. Also, the transient performance is better because one can design for a stable LDO with higher loop bandwidth. In addition,

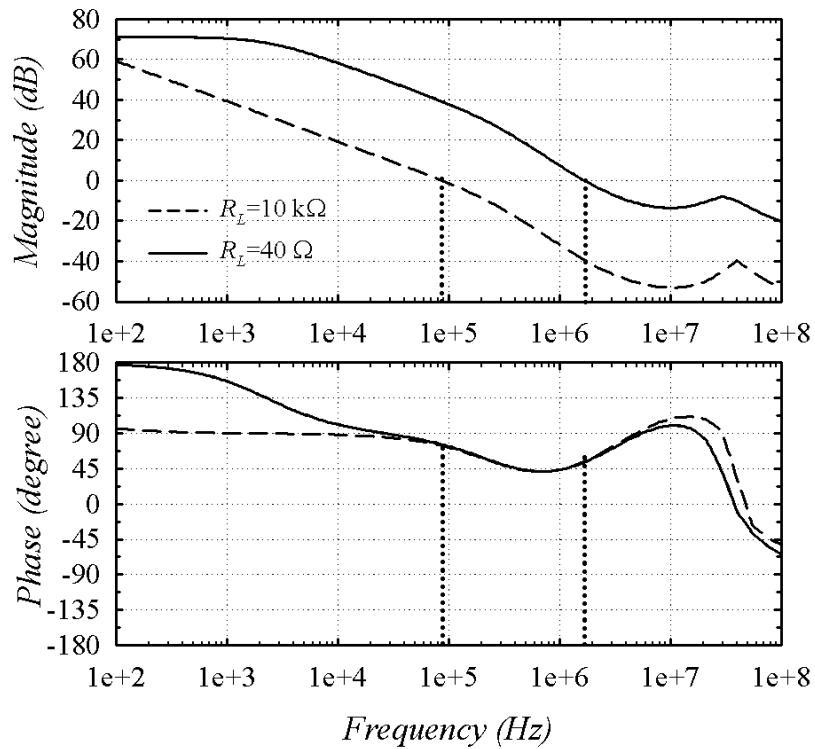


Fig. 103. Simulation of the open-loop gain and phase responses versus frequency of the LDO schematic using Kelvin connection for $R_L = 40 \, \Omega$ and $10 \, K\Omega$ ($L_b = 2 \, \text{nH}$, $C_L = 4 \, \mu\text{F}$, $L_c = 0.4 \, \text{nH}$, $R_{Lb} = 40 \, \text{m}\Omega$ per $1 \, \text{nH}$, $R_c = 30 \, \text{m}\Omega$, $R_{tot} = 14 \, \Omega$).

the extra inductor does not affect the transient load/line regulation because it does not appear along the high current variation path. Finally, an additional advantage of the Kelvin connection is better load regulation compared to the single bond-wire case because the output voltage is sensed after the voltage drop across the bond-wire resistance.

D. Circuit Implementation

The complete transistor-level implementation of the FFRC-LDO is shown in Fig. 104. The error amplifier utilizes current sources with improved output impedance as active loads [80]. This implementation boosts the output impedance of the amplifier through the feedback loop formed by transistors M_{3a} and M_{2a} . The resultant gain is higher than 55 dB. In addition, $PSRR_e$ exceeds 90 dB at DC to guarantee that the output PSR of the LDO is not limited by error amplifier as defined in (5.3). The capacitor, C_{c1} , is added to stabilize the internal feedback loop of the error amplifier. The gain and $PSRR_e$ schematic level simulations of the stand-alone error amplifier are shown in Fig. 105. The error amplifier achieves a 3-dB bandwidth of 180 kHz, and consumes a current of 12 μ A. This simulation shows that the PSR of the LDO does not depend on the bandwidth of the error amplifier when the FFRC technique is used. Process-voltage and temperature (PVT) variations showed a variation in the gain and $PSRR_e$ less than 5 dB.

The error amplifier has a limited output swing. This limited swing could be problematic for conventional LDOs when the error amplifier drives the pass transistor to accommodate a wide range of load currents. However in the presented LDO, the summing amplifier drives the gate of the pass transistor. The summing amplifier is implemented using a two stage amplifier configuration with resistive feedback, as shown in Fig. 104. A wide output swing is achieved from the second stage of this amplifier. The pass transistor gate capacitance is used to create the dominant pole of the amplifier, and hence, no additional capacitor is required to stabilize the amplifier. Without summing feedback resistances, the output pole exists at 500 kHz, and the internal non-dominant pole is at 28 MHz resulting in an amplifier phase margin of 45° . With the summing feedback resistances, the amplifier has a pole at 28 MHz, which is

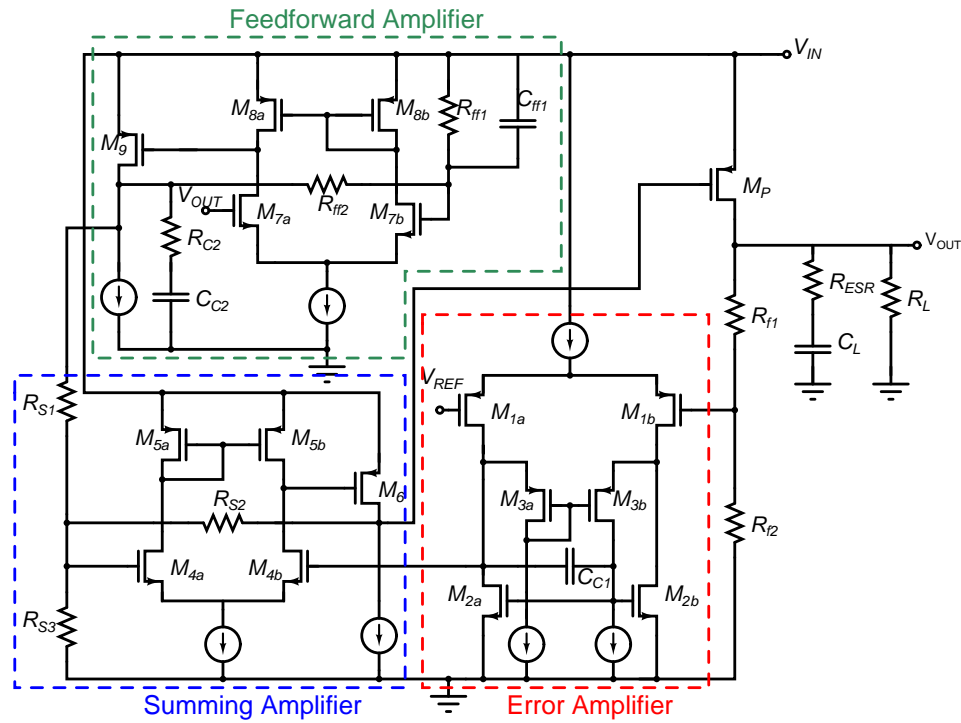


Fig. 104. Transistor-level implementation of the FFRC-LDO.

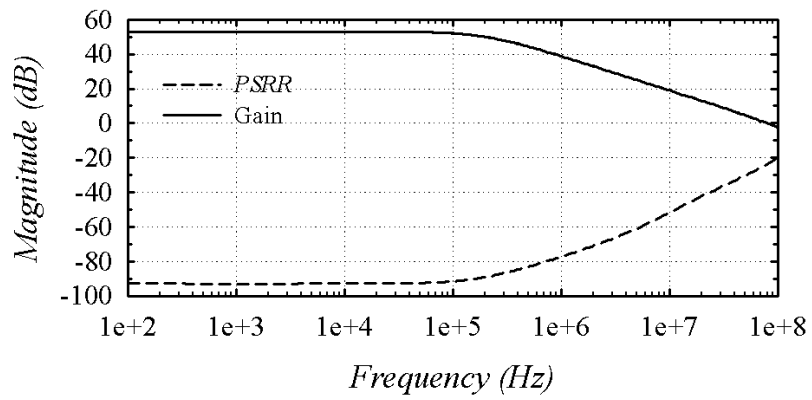


Fig. 105. Schematic level simulations of the gain and $PSRR_e$ of the error amplifier.

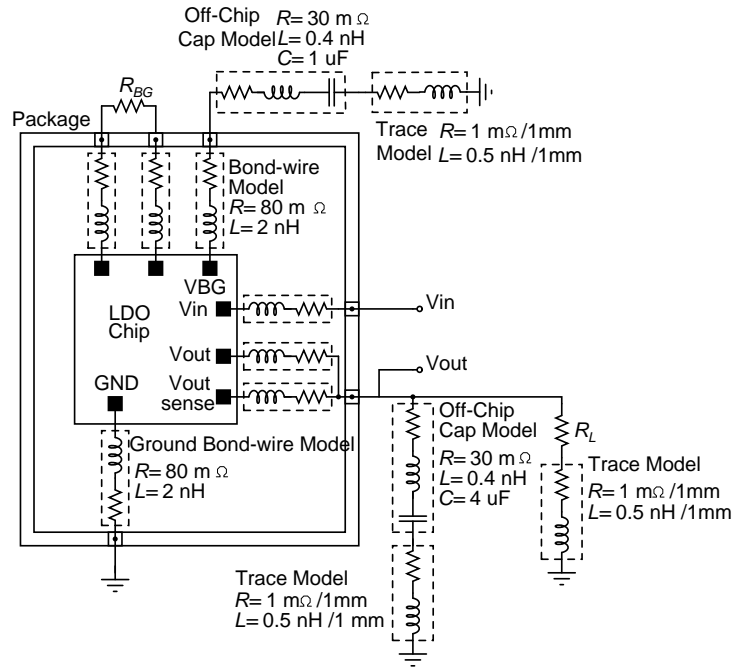


Fig. 106. Simulation setup of the FFRC LDO including the model of trace and off-chip capacitor parasitic models.

much higher than the GBW of the complete LDO. Therefore, the two stage topology does not affect the stability of LDO. As explained in Section III.B, the $PSRR$ of the summing amplifier is not critical in this design because the $PSRR$ is attenuated by the gain of the error amplifier. The feed-forward amplifier is also implemented using a two stage amplifier with resistive feedback. The capacitor, C_{c2} , and resistor, R_{c2} , are used to stabilize the amplifier. In this design, each of the summing and feed-forward amplifiers consumes a current of $13 \mu A$. The total on-chip capacitance that is used to compensate the amplifiers is less than $5 pF$.

The pass transistor is implemented using a PMOS device with minimum channel length and $2.4 mm$ width. Interdigitized and common centroid layout techniques are used to achieve high matching between the various resistors and transistors. Kelvin

connection is utilized to connect the LDO to the package to reduce the dependency on the bonding inductance. Two off-chip capacitors, each $2\ \mu\text{F}$, are used as the capacitive load of the LDO. During the design phase, the parasitic inductances, capacitances and resistances of the printed circuit board are also modeled to achieve simulations close to the measured performance as demonstrated in Fig. 106. The inductance and resistance of the traces are assumed to be $0.5\ \text{nH}$ and $1\ \text{m}\Omega$ per $1\ \text{mm}$, respectively. Without modeling these effects, the simulated PSR at high frequencies is not close to the one measured.

Bandgap voltage reference is used to generate the reference voltage of the LDO. Fig. 107 shows the implemented bandgap reference voltage circuit based on the architecture in [81]. The basic idea of this circuit is to replicate ripples at the gate of the current mirror (M_{1a} and M_{1b}), such that the output voltage is free from ripples. This is achieved through the transistors M_3 and M_4 [81]. The startup circuit is sized such that ripples leaking through the transistors do not affect the overall PSR of the bandgap circuit. An off-chip resistor is used for R_1 to adjust the required output voltage. The bandgap operates for a supply ranging from 1.15 to $1.8\ \text{V}$. The reference voltage, V_{ref} , is selected to be $0.5\ \text{V}$. This value is scaled to $1\ \text{V}$ through the feedback resistors, R_{f1} and R_{f2} . The bandgap circuit consumes a total current of $8\ \mu\text{A}$.

E. Experimental Results

The LDO is fabricated using $0.13\ \mu\text{m}$ CMOS technology provided through UMC. The chip is encapsulated in a Quad Flat No (QFN) leads package, and the chip micrograph is shown in Fig. 108. The total active area of LDO is $0.1\ \text{mm}^2$ including the bandgap circuitry. The bandgap circuit occupies around 50% of the total area. Two off-chip capacitors, each $2\ \mu\text{F}$, are used to stabilize the LDO. The off-chip load capacitor has

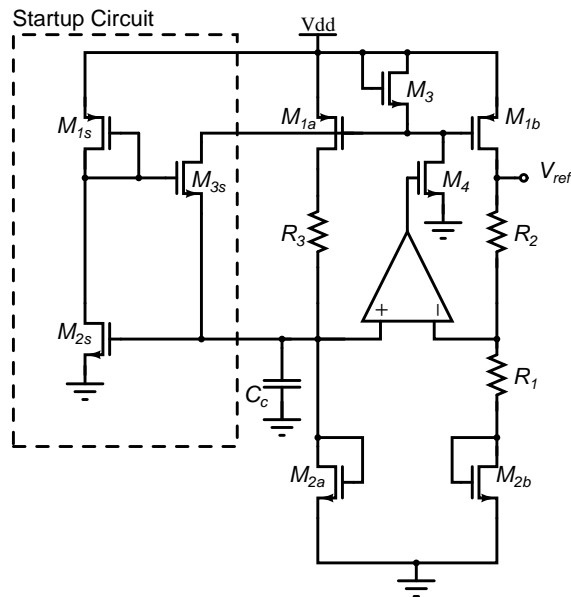


Fig. 107. Transistor-level implementation of the bandgap circuit.

an ESL and ESR of 400 pH and 10 m Ω , respectively. However, the effective ESL and ESR are higher due to the trace parasitics.

The total quiescent current of the LDO is 50 μ A at an input of 1.15V, where 8 μ A is consumed by the bandgap circuitry. The LDO operates for an input voltage ranging from 1.15 V to 1.8 V and the output voltage is 1 V. This shows a measured drop-out voltage of 0.15 V. The quiescent current depends on the input voltage and load current due to the DC path formed by summing and feed-forward resistances. At 1.8 V, the quiescent current increases by 6 μ A. It is important to note, that the biasing current of the second stage of summing and feed-forward amplifier should account for such current variations.

The *PSR* measurement setup is shown Fig. 109(a). The HP3588A spectrum analyzer with a high input impedance ($R_{in} = 1\text{ M}\Omega$) is used to measure the signal level at the input and output of the LDO. The *PSR* is measured by sweeping the

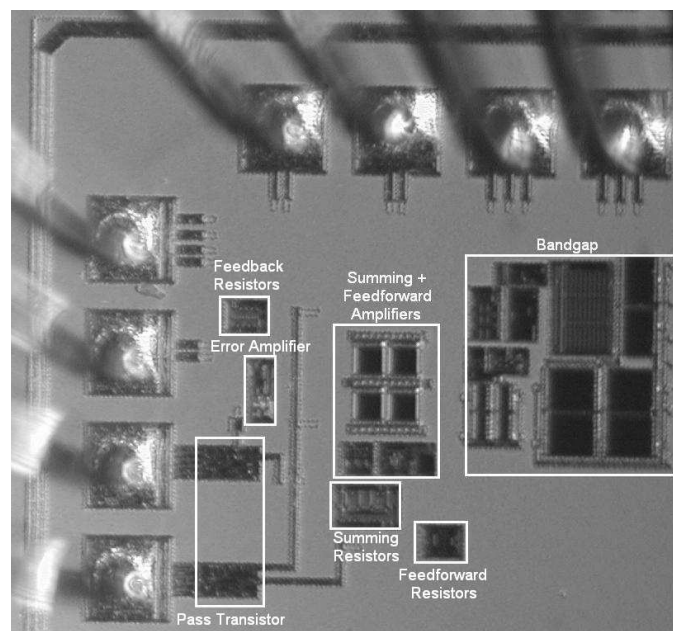


Fig. 108. Chip micrograph of the fabricated LDO with a total active area of 0.049 mm^2 including the bandgap circuitry.

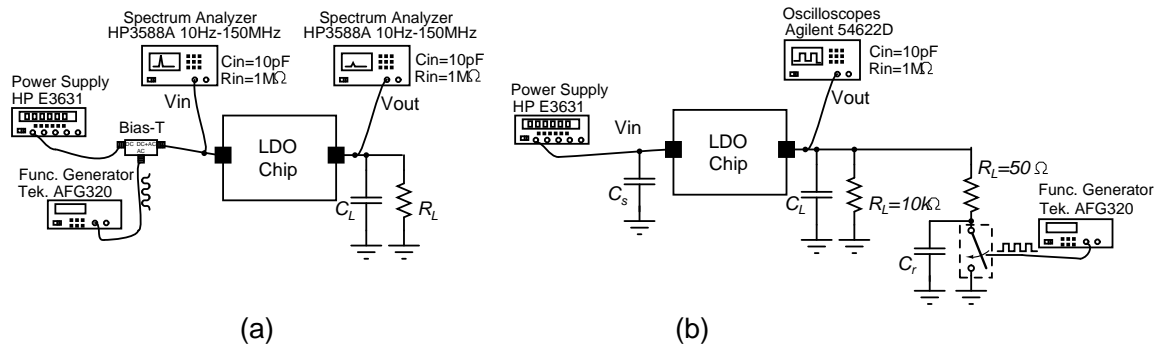


Fig. 109. Measurement setup for (a) *PSR* and (b) load transient measurements.

frequency of an input sine wave across the band of interest. The sine wave at the input of LDO is adjusted to 0.1 V at each measurement point. The measured *PSR* for different load currents is shown in Fig. 110 for a drop-out voltage of 0.15 V. The LDO achieves a worst *PSR* of -56 dB at 10 MHz for a load current of 25 mA. For frequencies above 4 MHz, the *PSR* starts to increase due to internal poles of the feed-forward and summing amplifiers. The *PSR* at a load current of 25 mA is worse than that at 5 mA because the pass transistor is operating near the triode region. In this case, the output conductance of the pass transistor is decreased, hence increases the *PSR*.

Increasing the drop-out voltage moves the operating point towards saturation, and a better *PSR* is achievable, as demonstrated in Fig. 111. For a conventional LDO with comparable performance at MHz frequencies, the open-loop gain and bandwidth should be increased, simultaneously. This increase comes at the cost of higher quiescent current as in [18], which is not the case using the FFRC technique.

The load transient response is measured using the setup shown in Fig. 109(b). A switch that is controlled by a clock, is used to switch the load current from the minimum to maximum load current. Capacitor C_r is added to control the rise time

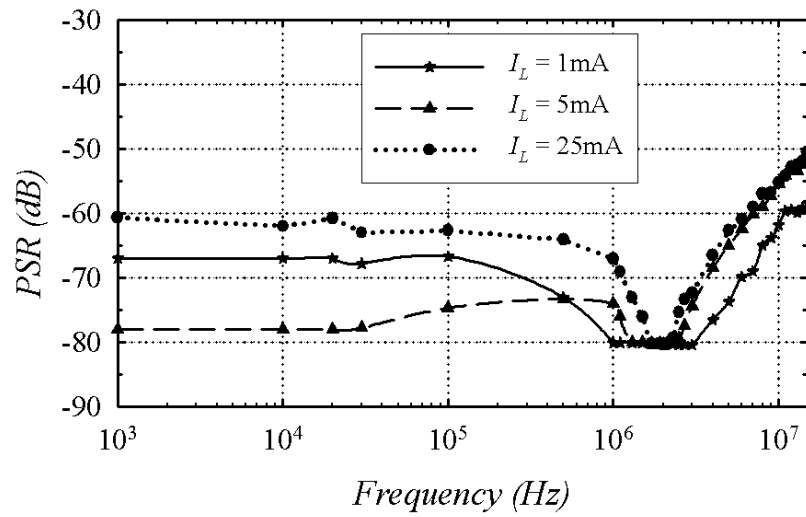


Fig. 110. Measured PSR for different load conditions (drop-out voltage = 0.15 V).

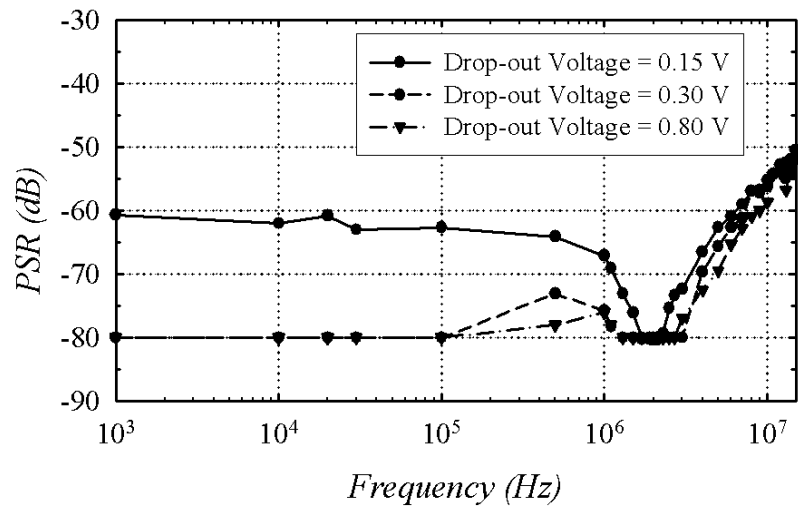


Fig. 111. Measured PSR for different drop-out voltage ($I_L = 25\text{mA}$).

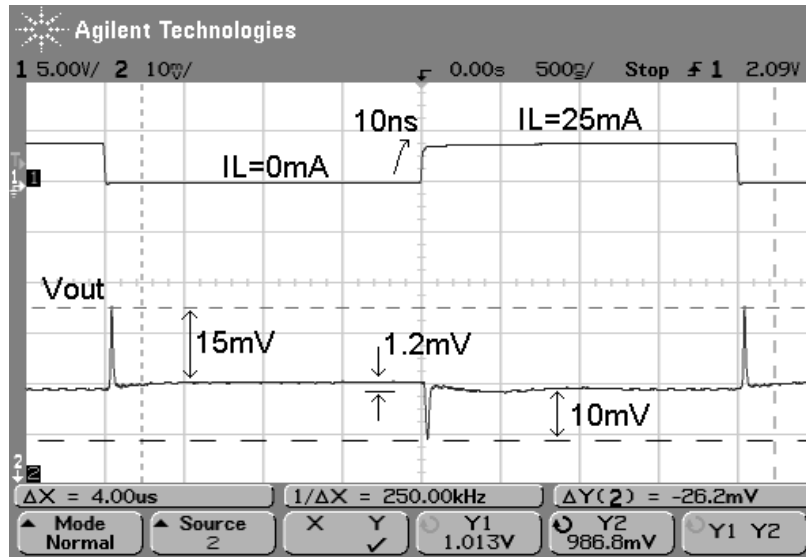


Fig. 112. Measured load transient response for a load current step of 25 mA.

of the load current. Capacitor C_s is added to guarantee a clean ground at the input of the LDO. Also, this capacitor shorts any inductive effect due to the measurement cables. Fig. 112 shows the measurement of the load transient response. A maximum overshoot of 15 mV is achieved for a 25 mA load current step with rise and fall times of 10 ns. The FFRC technique does not degrade the load transient response, when compared to [17], because the high-current path does not include any additional device for isolation other than the main pass transistor. Finally, the line transient response for an input that varies from 1.15 to 1.8 V shows a maximum variation of 1 mV at the output as shown in Fig. 113. A performance summary for the proposed FFRC-LDO and other existing architectures, which target high PSR LDOs, is summarized in Table XI.

Table XI. Performance summary of the proposed FFRC-LDO and comparison with the existing work.

	Unit	[16]	[17]	[18]	This Work
Tech.	(μm)	0.13	0.6	0.35	0.13
Active Area	mm^2	0.166	N.A.	0.053 ⁽³⁾	0.049 ⁽³⁾
V_{in}	V	3	>1.8	>1.05	>1.15
V_{out}	V	2.8	1.2	0.9	1
Drop-out Voltage	V	0.2	0.6	>0.15	>0.15
Max. Load Current	mA	150	5	50	25
Quiescent Current	μA	100 ⁽¹⁾	70 ⁽²⁾	80 @ 25mA 160 @ 50mA	50 ⁽⁴⁾
@ 100 kHz		-57	-70	-50	-60
PSR @ 1 MHz	dB	-40	-40	-50	-67
@ 10 MHz		N.A.	-27	N.A.	-56
Trans. Load Regulation	mV/mA	0.133	34.2	0.0614	0.048
$\Delta V_{out}/V_{out}$	mV/V	19.3/2.8	766/1.2	6.6/0.9	26/1

⁽¹⁾ Quiescent current for no-load condition. ⁽²⁾ Error amplifier and voltage reference only. ⁽³⁾ Without the bandgap circuit. ⁽⁴⁾ Overall quiescent current including amplifiers and bandgap voltage reference.

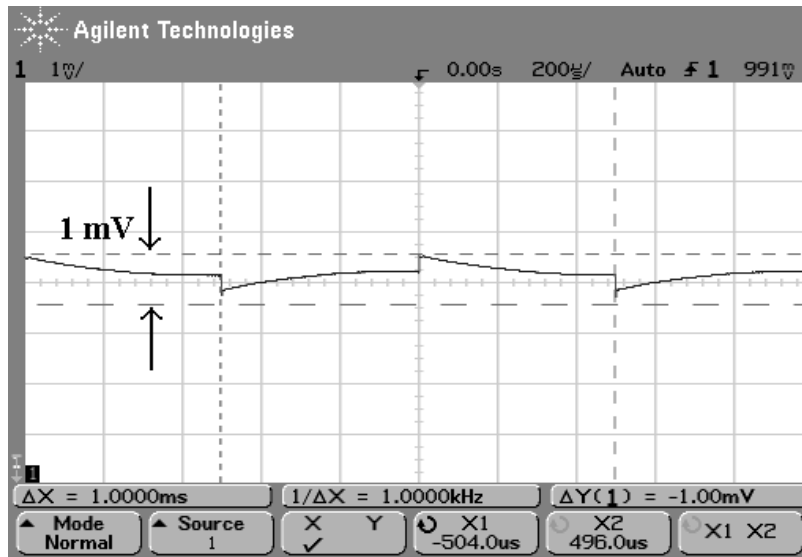


Fig. 113. Measured line transient response for an input step from 1.15 to 1.8 V and a load current 25 mA.

F. Summary

An LDO with a feed-forward ripple cancellation (FFRC) technique was proposed. The proposed topology provides a robust design when the process, temperature and bonding inductance variations are considered. The FFRC can be extended to any existing LDO architecture to yield a high PSR for a wide range of frequencies. A fabricated prototype of the FFRC-LDO achieved a power-supply-rejection (PSR) better than -56 dB up to 10 MHz. To our knowledge, this is the first LDO that achieves this high PSR up to 10 MHz. A complete analysis of PSR for the FFRC and the conventional LDO were presented. In addition, it was shown that Kelvin connection at the output helps to increase the GBW of the LDO without affecting the stability at heavy loads. The LDO was implemented in $0.13\ \mu\text{m}$ CMOS technology and occupies an area of $0.049\ \text{mm}^2$. Measurements showed a load regulation of 1.2 mV for a 25 mA step current, and the whole LDO consumed a quiescent current of $50\ \mu\text{A}$.

with a bandgap reference circuit included.

CHAPTER VI

CONCLUSIONS

The design and implementation methodologies for multi-band / multi-standard (MB/MS) mobile units that target high data rate while consuming minimum power consumption is discussed in this dissertation. The dissertation covers various aspects of MB/MS receivers and their building blocks including system-level design, novel architectures of the receiver, wideband building blocks for mm-wave frequency range, a reconfigurable low noise amplifier, and a low-drop out regulator with high power supply rejection. The proposed research methodology promises significant improvement in power budgeting and is realizable by the aid of low-cost silicon-based technologies.

The first part of the dissertation discusses a systematic system-level design approach for block-level budgeting to minimize the power consumption. This methodology is generalized for MB-MS receiver, and analytical expressions for NF and V_{IIP3}^2 of each building block are provided. Also, it is shown that the gain variation of the LNA for different standards/bands is an important factor which determines the power consumption. The methodology is tested for a wideband receiver covering GSM-900, GSM-1900, GPS and WCDMA standards. As an example, the power consumption is reduced by 40% when compared to the approach where the gain of the LNA is kept constant. This system-level design methodology enables the design of the optimum receiver without relying on the experience of the designer, hence reducing the design cycle.

This methodology is applied to a novel dual-band receiver. The receiver relies on a new concept for band selection through switching between the harmonics of the down-conversion mixer. The receiver is implemented for the ISM and LMDS bands at 24 and 31 GHz, and targeting the IEEE 802.16 standard. Mathematical formulation

and frequency planning of the receiver is also provided. A prototype is fabricated using $0.18\ \mu\text{m}$ BiCMOS technology with $0.7\ \text{mm}^2$ of chip area. Measurements shows a band rejection higher than 43 dB, gain higher than 14 dB, NF lower than 11 dB, and IIP3 higher than -16 dBm. The receiver consumes 60 mW from a 1.8 V supply. The new concept of dual-band down-conversion enables the designer to reuse the various building blocks, and therefore, reduce the area consumption and complexity of the receiver.

The novel dual-band receiver depends on new wideband circuit techniques for the LNA and mm-wave mixer. Through the concept of coupled load resonators, a wideband LNA is implemented at mm-wave frequencies. In addition, a peaking technique is applied to the sub-harmonic mm-wave mixer to extend its bandwidth. Proposed methodologies enable wideband building blocks (LNA and mm-wave mixer) to achieve the highest reported bandwidth for silicon-based technologies. The theory behind each methodology is presented in the dissertation along with analytical expressions for main performance parameters. A separate prototype is fabricated using $0.18\ \mu\text{m}$ BiCMOS technology to prove the concept. The LNA shows a constant gain across 23-32 GHz frequency range, while the sub-harmonic mm-wave mixer provides a 20-32 GHz operating range and IF bandwidth of 12 GHz.

Another topic discussed in this dissertation is the design of an LNA with reconfigurable input matching network by means of a new technique to tune the inductance value. A design methodology for minimizing the power consumption of the additional tuning circuit is also presented. This methodology is used to design and implement a reconfigurable LNA along the frequency band of 1.9-2.4 GHz. The $0.13\ \mu\text{m}$ CMOS technology is employed to implement the LNA, which consumes 14 mA from a 1.2 V supply. Measured performance shows an input matching better than -13 dB, a voltage gain of 10-14 dB, and a noise figure of 3.2-3.7 dB over the tuning range. This tuning

scheme demonstrates the first technique for continuous tuning of the input matching network. The proposed technique is not only suitable for tuning the matching network, but can be generally used to scale the inductance value for any application.

Finally, an LDO with a feed-forward ripple cancellation (FFRC) technique is presented. The proposed topology provides a robust design when the process, temperature and bonding inductance variations are considered. The FFRC can be extended to any existing LDO architecture to yield a high PSR for a wide range of frequencies. A fabricated prototype of the FFRC-LDO achieves a power-supply-rejection (PSR) better than -56 dB up to 10 MHz. The complete analysis of PSR for the FFRC and the conventional LDO are presented. In addition, it is shown that Kelvin connection at the output helps to increase the GBW of the LDO without affecting the stability at heavy loads. The LDO is implemented using 0.13 μm CMOS technology.

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